

Stanford 11"

CPU : C-ULV
Chip Set : CANTIGA GS & ICH9M SFF
Remarks : INTEL MONTEVINA SFF

Model Name : Stanford_DDR3
PCB Part No : BA41-01150A(GCE)
BA41-01151A(NANYA)
Dev. Step : MP
Revision : 1.0
T.R. Date : 2009.07.31

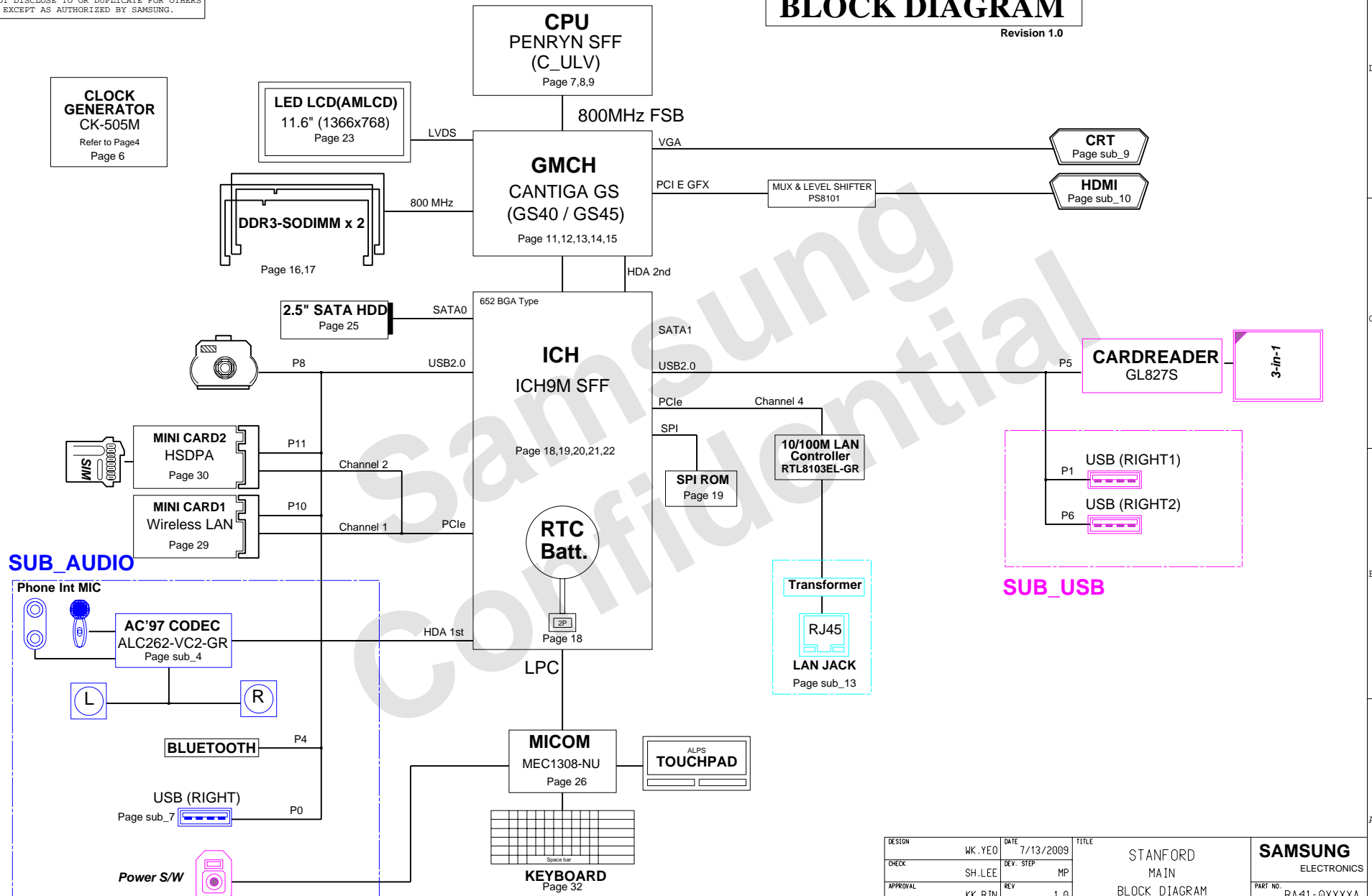
DRAW	CHECK	APPROVAL

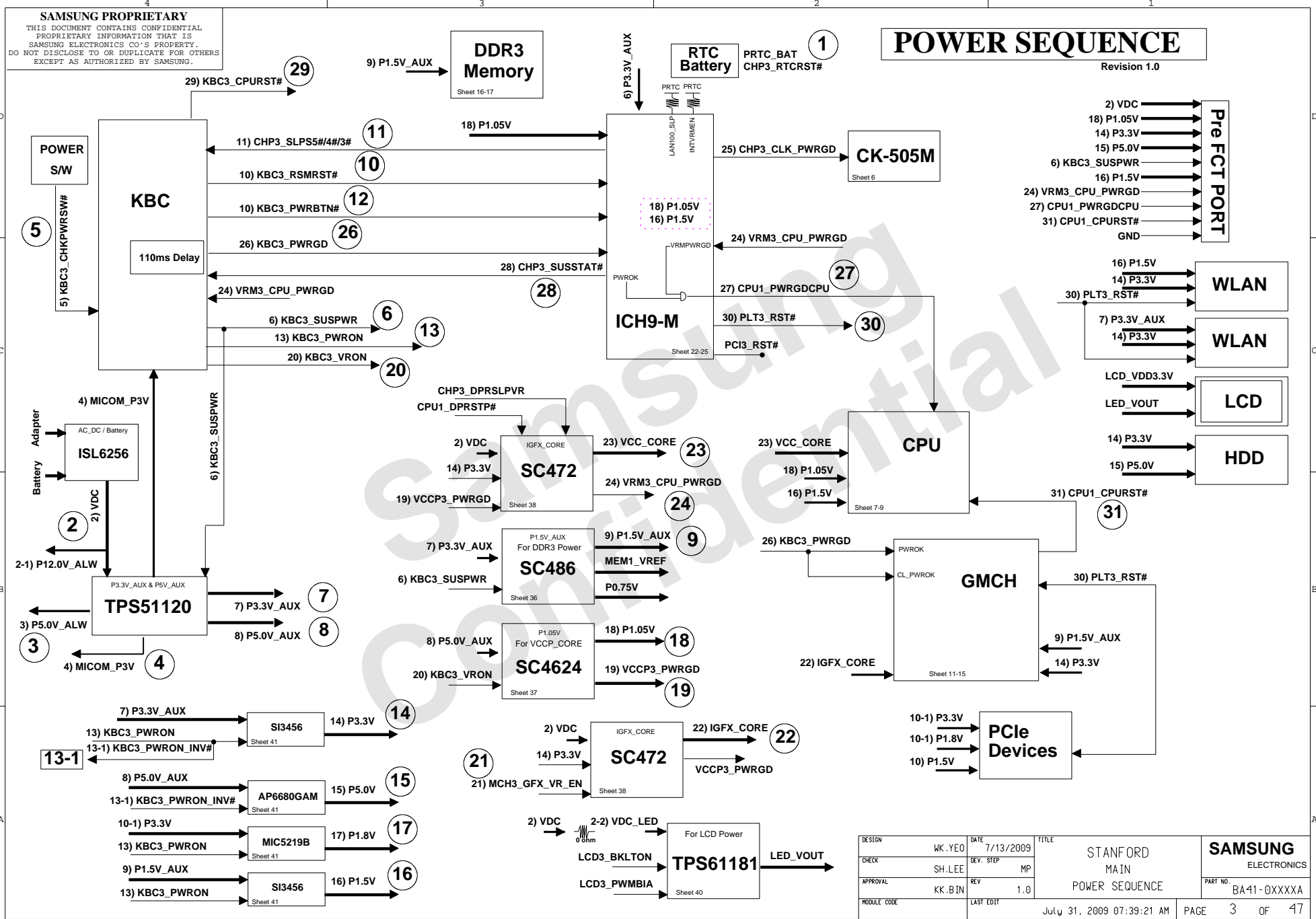
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DESIGN	WK.YEO	DATE	7/13/2009	TITLE	STANFORD MAIN COVER	SAMSUNG ELECTRONICS
CHECK	SH.LEE	DEV. STEP	MP			PART NO. BA41-0XXXXA
APPROVAL	KK.BIN	REV	1.0			
MODULE CODE		LAST EDIT	July 31, 2009 07:39:21 AM	PAGE	1	OF 47

Revision 1.0





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POWER SEQUENCE

Revision 1.0

- Pre FCT PORT**
- 2) VDC
 - 18) P1.05V
 - 14) P3.3V
 - 15) P5.0V
 - 6) KBC3_SUSPWR
 - 16) P1.5V
 - 24) VRM3_CPU_PWRGD
 - 27) CPU1_PWRGDCPU
 - 31) CPU1_CPURST#
 - GND

- WLAN**
- 16) P1.5V
 - 14) P3.3V
 - 7) P3.3V_AUX
 - 14) P3.3V
- WLAN**
- 7) P3.3V_AUX
 - 14) P3.3V
- LCD**
- LCD_VDD3.3V
 - LED_VOUT
- HDD**
- 14) P3.3V
 - 15) P5.0V

DESIGN	WK.YEO	DATE	7/13/2009	TITLE	STANFORD MAIN POWER SEQUENCE	SAMSUNG ELECTRONICS	
CHECK	SH.LEE	REV. STEP	MP				PART NO. BA41-0XXXXA
APPROVAL	KK.BIN	REV	1.0				
MODULE CODE	LAST EDIT		July 31, 2009 07:39:21 AM				

Revision 1.0



DESIGN	WK.YE0	DATE	7/13/2009	TITLE STANFORD MAIN CLOCK DISTRIBUTION			SAMSUNG ELECTRONICS		
CHECK	SH.LEE	REV. STEP	MP						
APPROVAL	KK.BIN	REV	1.0						
MODULE CODE	LAST EDIT								July 31, 2009 07:39:21 AM
							PART NO.		BA41-0XXXXA

BOARD INFORMATION

SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

PCI Devices

Devices	IDSEL#	REQ/GNT#	Interrupts
USB LPC Bridge/IDE/AC97/SMBUS Internal MAC	AD29(internal) AD31(internal) AD24(internal)	Programmable	

I²C / SMB Address

Devices	Address	Hex	Bus
ICH9M	Master		SMBUS Master
CK-505M (Clock Generator)	1101 001X	D2h	Clock, Unused Clock Output Disable
SODIMM0	1010 000X	A0h	-
SODIMM1	1010 001X	A4h	-
PI3HDMI412AD	1010 001X	C0h	-
MICOM	Master		
BATTERY	0001 011X	16h	-
EMC2102	0111 101X	7Ah	-

USB PORT Assign

Port Number	ASSIGNED TO	Port Number	ASSIGNED TO
UHCL_0 0	USB PORT (LEFT)	UHCL_3 6	USB PORT (RIGHT2)
2	USB PORT (RIGHT1)	7	EXPRESS CARD
UHCL_1 3	USB HUB1 (DOCK)	UHCL_4 9	CAMERA
4	USB HUB2 (DOCK)	10	FINGER PRINT
UHCL_2 5	BLUETOOTH	UHCL_5 11	WLAN for Combo
	AU6371		HSDPA

System Power States

Power Rail	Devices (Page Number)
P5.0V	EMC2102 (10) ICH9M (21) 1.8" SATA HDD (25) MICOM (26) Pre FCT PORT (32) DISCHARGE, CAMERA, TOUCHPAD (33) SC472 (38) SC454 (39) AP6680 (41) P15V330QX (24,42) HDMI CONN. (SUB_10) CRT CONN. (SUB_9)
P3.3V	CK505M (6) FAN (10) CANTIGA GS (14) SPI ROM (19) ICH9M (21) LED LCD (23) 1.8" SATA HDD (25) WLAN (29) HSDPA (30) PI3HDMI412AD (31) Pre FCT PORT (32) DEBUG PORT, Pre FCT PORT & WHITE LED (32) DISCHARGE & BLUETOOTH (33) SWITCHED (41) LPC47N207 (43) ALC262-VC2 (SUB_4) R5538 (SUB_7) POWER S/W LED (SUB_11) AU6371 (SUB_12) AES1610 (SUB_14)
P1.8V	CANTIGA GS (14) DISCHARGE (33) SWITCHED (41)
P1.5V	CK505M (6) PENRYN ULV (8) CANTIGA GS (14) ICH9M (21) WLAN (29) HSDPA (30) Pre FCT PORT (32) DISCHARGE (33) SWITCHED (41) ALC262-VC2 (SUB_4) R5538 (SUB_7)
P1.05V	PENRYN ULV (8) CANTIGA GS (11,14) ICH9M (21) Pre FCT PORT (32) DISCHARGE (33) SC4624 (37)
P0.75V	DDR3 (16, 17) SC486 (36)
P5V_AUX	ICH9M (21) TPS51120 (35) SC486 (36) SC4624 (37) SWITCHED (41) USB PORT (7,11)
P3.3V_AUX	EMC2102 (10) ICH9M (21) 88E8055 (27) STMUX1000 (28) WLAN (29) LAN JACK LED (32) TPS51120 (35) SWITCHED (41) SLB9635 (43) R5538 (SUB_7)
P1.5V_AUX	CANTIGA GS (14) DDR3 (16, 17) ICH9M (21) SC486 (36) SWITCHED (41)
VCC_CORE	PENRYN ULV (8,9) SC454 (39)
VCC_CORE	CANTIGA GS (12)

Voltage Rails

Power Rail	Descriptions	Power Rail	Descriptions
AD_DC VDC	Primary DC system power supply (9 to 19V)	P1.05V_PEG	P1.05V (Direct Media Interface Compensation)
CHG_REF	Charger Reference Voltage Source	P5.0V	5.0V Power Rail (off in S3-S5)
PRTC_BAT	3.3V supply for the RTC well.	P3.3V	3.3V Power Rail (off in S3-S5)
P5.0V_FILT	???	P1.8V	1.8V Power Rail (off in S3-S5)
P12.0V_ALW	???	P1.5V	1.5V Power Rail (off in S3-S5)
P5.0V_ALW	???	P1.05	1.05V Power Rail (off in S3-S5)
		P0.75V	DDR3 Termination
		P5.0V_AUX	5.0V Power Rail (off in S4-S5)
		P3.3V_AUX	3.3V Power Rail (off in S4-S5)
		P1.5V_AUX	1.5V Power Rail (off in S4-S5)
		VCC_CORE	Core Voltage for PENRYN ULV
		IGFX_CORE	Core Voltage for CANTIGA GS
MICOM_P3V	Output voltage of ISL6256(Charger) (if VDC is removed, it will be off)		
LCD_VDD3V	3.3V (LED LCD)	AUD_P5V	5.0V switched power rail (off in S3-S5)
LED_VOUT	7V-19V (LED LCD)	AMP_VDD	5.0V (Audio AMP)
VDC_LED	VDC (LED LCD)	AVDD	5.0V (ADI1986)
P5.0V_CRT	5.0V (CRT Conn.)		
VCC_CRT	5.0V (CRT)	P1.5V_EXT	1.5V (R5538, EXPRESS CARD)
		P3.3V_AUX_EXT	3.3V (R5538, EXPRESS CARD)
P1.2V_LAN		P3.3V_EXT	
P1.8V_P2.5V_LAN	Internal Regulator's Power of LAN Controller		
		3.3V_VDD	3.3V (AES1610, FINGER PRINT)
P3.3V_MCD	3.3V (7-in-1 Socket)	FP_P3.3V	3.3V (AES1610, FINGER PRINT)

CPU Core Voltage Table

VID6	VID5	VID4	VID3	VID2	VID1	VID0	Voltage	VID6	VID5	VID4	VID3	VID2	VID1	VID0	Voltage	VID6	VID5	VID4	VID3	VID2	VID1	VID0	Voltage
0	0	0	0	0	0	0	1.5000	0	1	0	0	0	0	0	1.1000	1	0	0	0	0	0	0	0.7000
0	0	0	0	0	0	1	1.4875	0	1	0	0	0	0	1	1.0875	1	0	0	0	0	0	1	0.6875
0	0	0	0	0	1	0	1.4750	0	1	0	0	0	1	0	1.0750	1	0	0	0	0	1	0	0.6750
0	0	0	0	0	1	1	1.4625	0	1	0	0	0	1	1	1.0625	1	0	0	0	0	1	1	0.6625
0	0	0	0	1	0	0	1.4500	0	1	0	0	1	0	0	1.0500	1	0	0	0	1	0	0	0.6500
0	0	0	0	1	0	1	1.4375	0	1	0	0	1	1	0	1.0375	1	0	0	0	1	0	0	0.6375
0	0	0	0	1	1	0	1.4250	0	1	0	0	1	1	1	1.0250	1	0	0	0	1	1	0	0.6250
0	0	0	0	1	1	1	1.4125	0	1	0	0	1	1	1	1.0125	1	0	0	0	1	1	1	0.6125
0	0	0	1	0	0	0	1.4000	0	1	0	0	1	0	0	1.0000	1	0	0	0	1	0	0	0.6000
0	0	0	1	0	0	1	1.3875	0	1	0	0	1	0	1	0.9875	1	0	0	0	1	0	1	0.5875
0	0	0	1	0	1	0	1.3625	0	1	0	0	1	0	1	0.9750	1	0	0	0	1	1	0	0.5750
0	0	0	1	1	0	0	1.3500	0	1	0	0	1	0	1	0.9625	1	0	0	0	1	1	1	0.5625
0	0	0	1	1	0	1	1.3375	0	1	0	0	1	0	1	0.9500	1	0	0	0	1	1	1	0.5500
0	0	0	1	1	1	0	1.3250	0	1	0	0	1	0	0	0.9375	1	0	0	0	1	1	1	0.5375
0	0	0	1	1	1	1	1.3125	0	1	0	0	1	1	0	0.9250	1	0	0	0	1	1	1	0.5125
0	0	0	1	0	0	0	1.3000	0	1	0	0	1	1	1	0.9125	1	0	0	0	1	1	0	0.5000
0	0	0	1	0	0	1	1.2875	0	1	0	0	1	1	1	0.9000	1	0	0	0	1	1	0	0.4875
0	0	0	1	0	0	1	1.2750	0	1	0	0	1	0	0	0.8875	1	0	0	0	1	0	0	0.4750
0	0	0	1	0	1	0	1.2625	0	1	0	0	1	0	1	0.8750	1	0	0	0	1	0	1	0.4625
0	0	0	1	0	1	1	1.2500	0	1	0	0	1	0	1	0.8625	1	0	0	0	1	0	1	0.4500
0	0	0	1	0	1	1	1.2375	0	1	0	0	1	0	0	0.8500	1	0	0	0	1	0	1	0.4375
0	0	0	1	0	1	1	1.2250	0	1	0	0	1	0	0	0.8375	1	0	0	0	1	0	1	0.4250
0	0	0	1	0	1	1	1.2125	0	1	0	0	1	0	0	0.8250	1	0	0	0	1	0	1	0.4125
0	0	0	1	0	0	0	1.2000	0	1	0	0	1	1	0	0.8125	1	0	0	0	1	0	0	0.4000
0	0	0	1	0	0	1	1.1875	0	1	0	0	1	1	1	0.8000	1	0	0	0	1	0	0	0.3875
0	0	0	1	0	1	0	1.1750	0	1	0	0	1	0	0	0.7875	1	0	0	0	1	0	0	0.3750
0	0	0	1	0	1	1	1.1625	0	1	0	0	1	0	1	0.7750	1	0	0	0	1	0	0	0.3625
0	0	0	1	0	1	1	1.1500	0	1	0	0	1	0	1	0.7625	1	0	0	0	1	0	0	0.3500
0	0	0	1	0	1	1	1.1375	0	1	0	0	1	0	1	0.7500	1	0	0	0	1	0	0	0.3375
0	0	0	1	0	1	1	1.1250	0	1	0	0	1	0	0	0.7375	1	0	0	0	1	0	0	0.3250
0	0	0	1	0	1	1	1.1125	0	1	0	0	1	0	0	0.7250	1	0	0	0	1	0	0	0.3125
								0	1	1	1	1	1	1	0.7125	1	0	0	0	1	0	0	0.3000

Active Mode

Active / Deeper Sleep Dual Mode

Deeper Sleep / Deep Power Down Mode

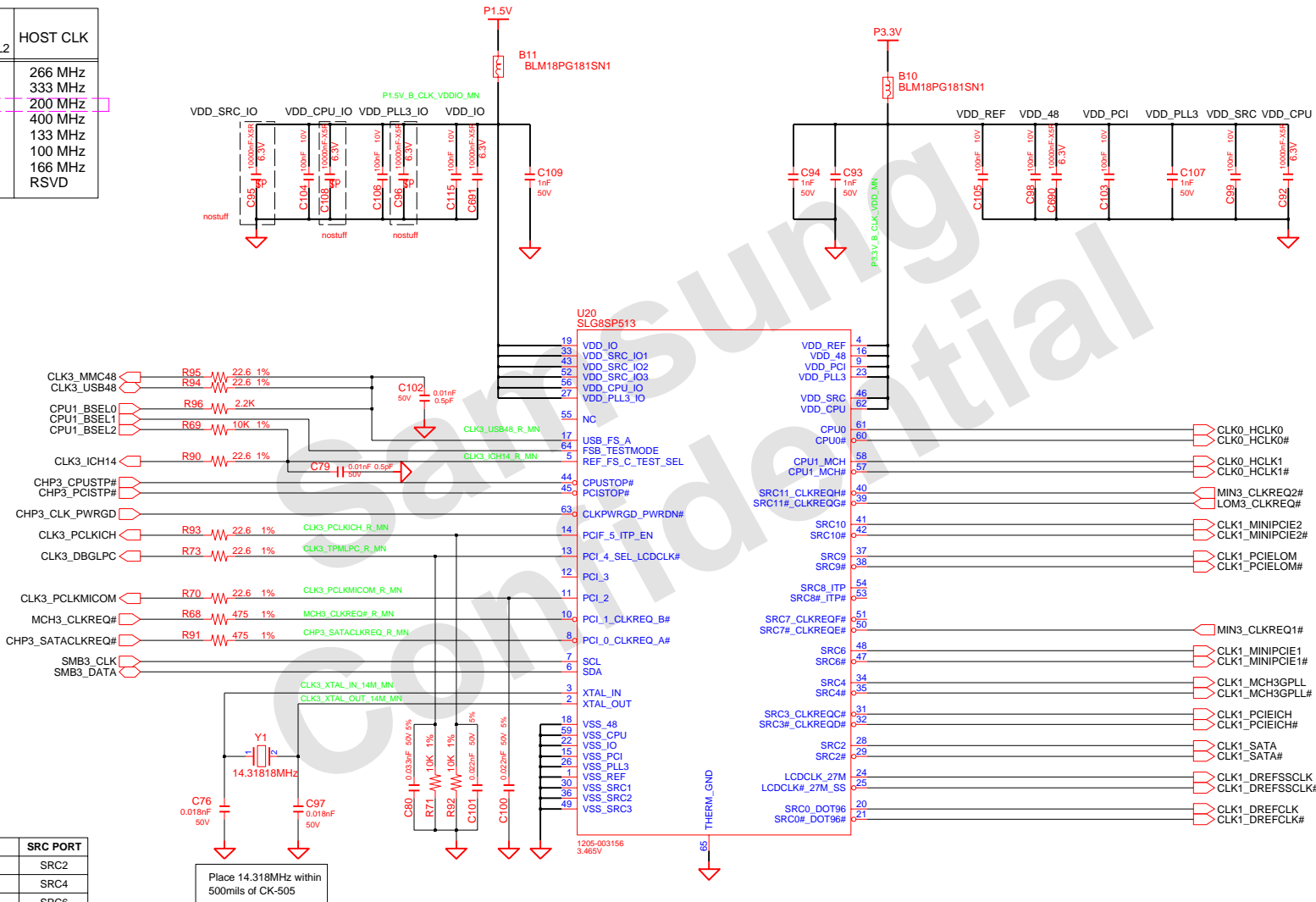
Programmable Deep Power Down

GMCH Core Voltage

EN	V4	V3	V2	V1	V0	Voltage
1	0	0	0	0	0	1.250
1	0	0	0	0	1	1.225
1	0	0	0	1	0	1.200
1	0	0	0	1	1	1.175
1	0	0	1	0	0	1.150
1	0	0	1	0	1	1.125
1	0	0	1	1	0	1.100
1	0	0	1	1	1	1.075
1	0	1	0	0	0	1.050
1	0	1	0	0	1	1.025
1	0	1	0	1	0	1.000
1	0	1	0	1	1	0.975
1	0	1	1	0	0	0.950
1	0	1	1	0	1	0.925
1	0	1	1	1	0	0.900
1	0	1	1	1	1	0.875
1	1	0	0	0	0	0.850
1	1	0	0	0	1	0.825
1	1	0	0	1	0	0.800
1	1	0	0	1	1	0.775
1	1	0	1	0	0	0.750
1	1	0	1	0	1	0.725
1	1	0	1	1	0	0.700
1	1	0	1	1	1	0.675
1	1	1	0	0	0	0.650
1	1	1	0	0	1	0.625
1	1	1	0	1	0	0.600
1	1	1	0	1	1	0.575
1	1	1	1	0	0	0.550
1	1	1	1	0	1	0.525
1	1	1	1	1	0	0.500
1	1	1	1	1	1	0.400
0	0	X	X	X	X	0.000

Render Performance States
Render Suspend States


FSA BSEL0	FSB BSEL1	FSC BSEL2	HOST CLK
0	0	0	266 MHz
0	0	1	333 MHz
0	1	0	200 MHz
0	1	1	400 MHz
1	0	0	133 MHz
1	0	1	100 MHz
1	1	0	166 MHz
1	1	1	RSVD



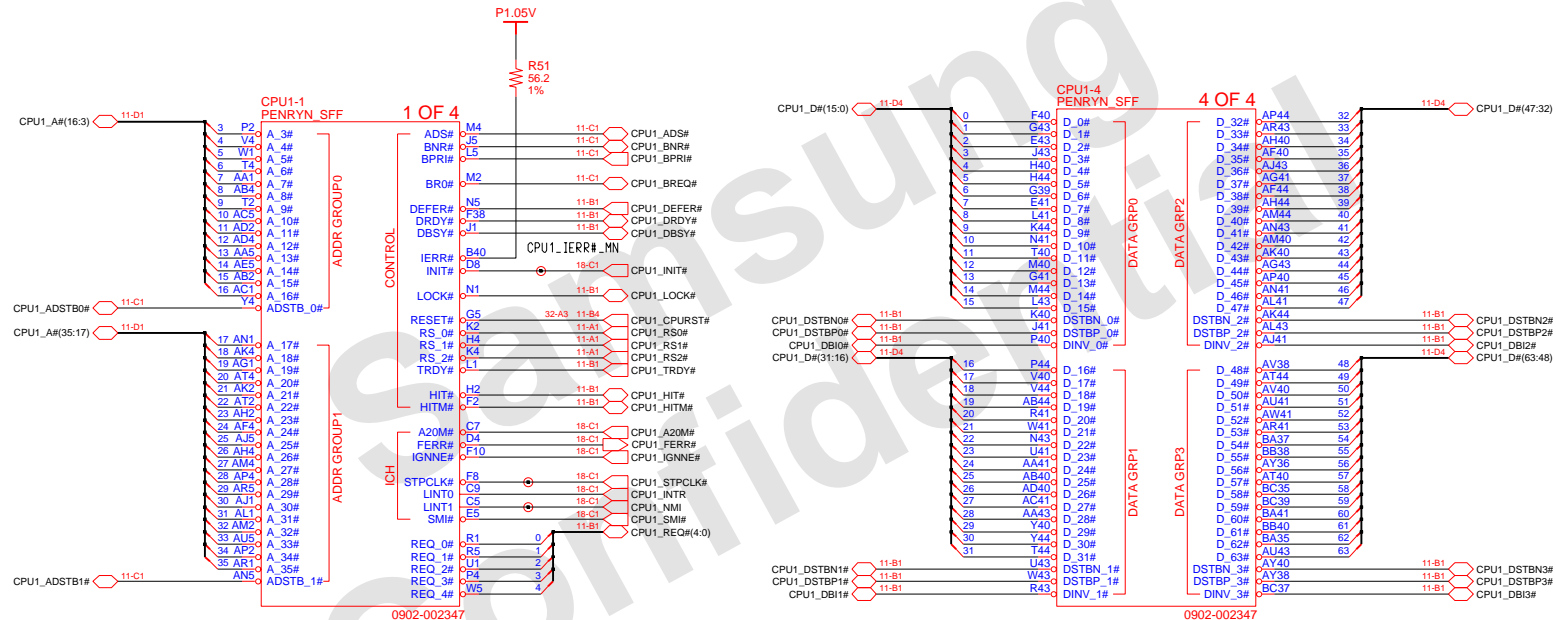
CLK REQ	DEVICE	SRC PORT
CLK REQ A	SATA	SRC2
CLK REQ B	GMCH	SRC4
CLK REQ E	MINI CARD	SRC6
CLK REQ F	EXP3_CLKREQ#	SRC8

SEL_LCDCLK*	Pin 20/21	Pin 24/25
LOW	DOT_96/DOT_96#	PEG_CLK/PEG_CLK#

This part is 64pin QFN package.

DESIGN	WK.YEO	DATE	7/13/2009	TITLE		STANFORD MAIN CLOCK GENERATOR	
CHECK	SH.LEE	DEV. STEP	MP				
APPROVAL	KK.BIN	REV	1.0	LAST EDIT		July 31, 2009 07:39:21 AM	PART NO. BA-01-0XXXXA PAGE 6 OF 47
MODULE CODE							

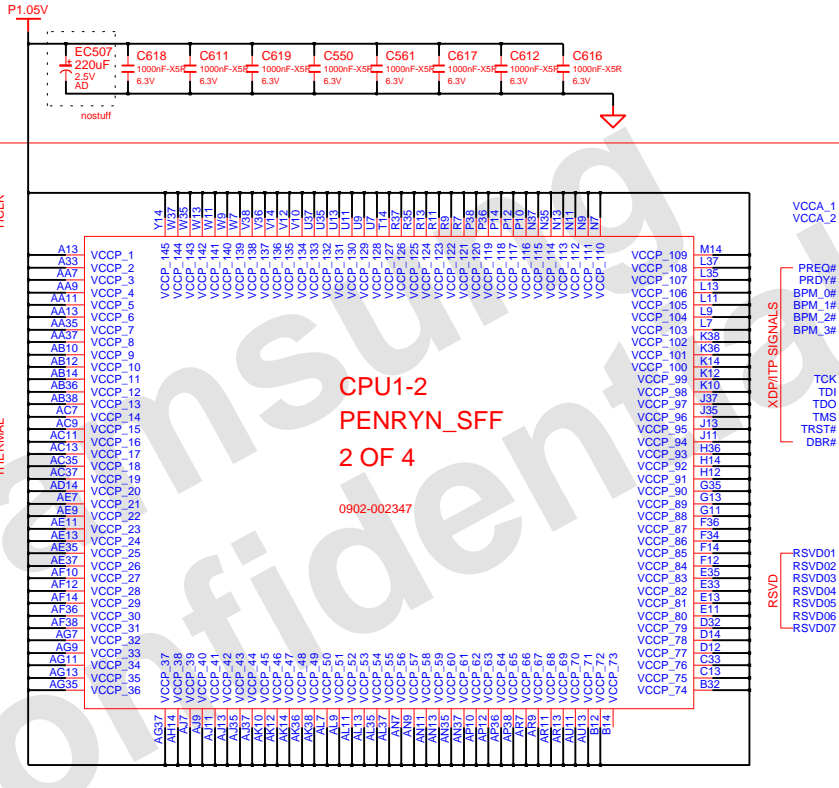
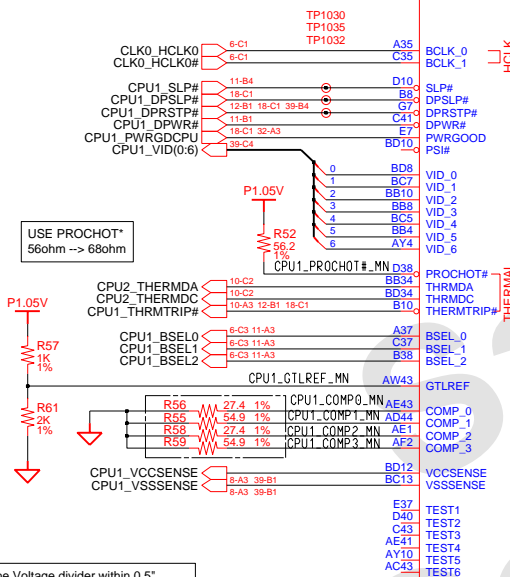
ULV CPU(Penryn SFF)



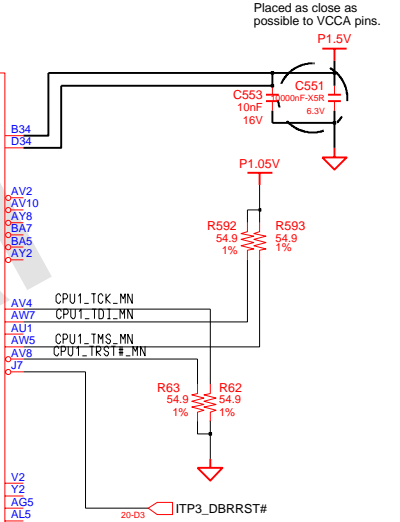
DESIGN	WK.YEO	DATE	7/13/2009	TITLE		<div style="text-align: center;"> STANFORD MAIN PENRYN ULV CPU(1/3) </div>		<div style="text-align: center;"> SAMSUNG ELECTRONICS </div>	
CHECK	SH.LEE	DEV. STEP	MP						
APPROVAL	KK.BIN	REV	1.0	<div style="text-align: center;"> PENRYN ULV CPU(1/3) </div>		PART NO.		BA41-0XXXXA	
MODULE CODE		LAST EDIT							
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ULV CPU(Penryn SFF)

GTLREF : Keep the Voltage divider within 0.5"
of the first GTLREF0 pin with Zo=55ohm trace.
Minimize coupling of any switching signals to this net.



CPU1-2
PENRYN_SFF
2 OF 4
0902-002347

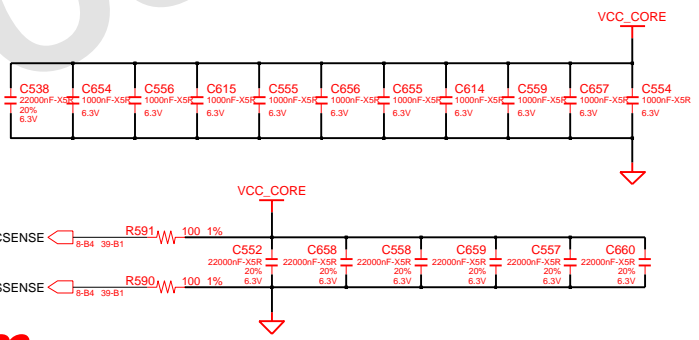


GTLREF : Keep the Voltage divider within 0.5"
of the first GTLREF0 pin with Zo=55ohm trace.
Minimize coupling of any switching signals to this net.

COMP0,2(COMP1,3) should be connected with Zo=27.4ohm(55ohm)
trace shorter than 1/2" to their respective Banias socket pins.

GND test points within 100mil of the VCC/VSSense at the end of the line.
Route the VCC/VSSense as a Zo=55ohm traces with equal length.
Observe 3:1 spacing b/w VCC/VSSense lines and 25mil away
(preferred 50mil) from any other signal. And GND via 100mil away
from each of the VCC/VSS test point vias.

VCC/VSSense lines between the Penryn CPU and the VR
should have a trace width of 18mils on 7mil spacing
with trace impedance of Zo=27.4ohm
Place PU and PD within 1 inch of CPU

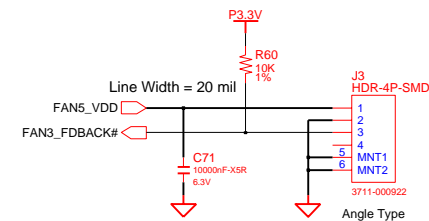
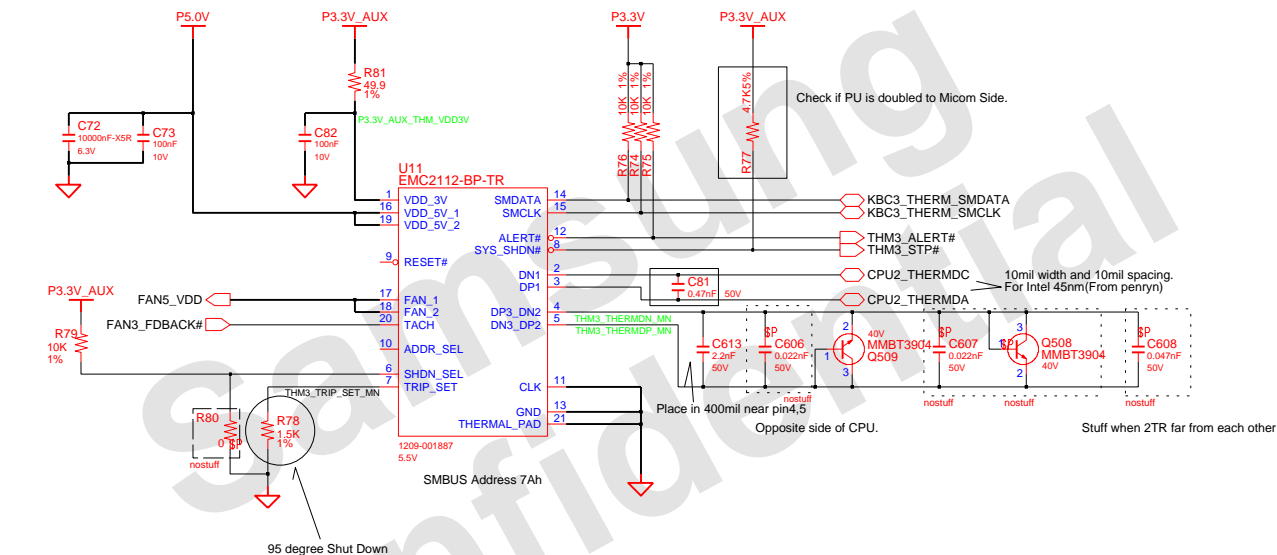


DESIGN	WK.YEO	DATE	7/13/2009	TITLE	STANFORD MAIN	SAMSUNG ELECTRONICS
CHECK	SH.LEE	DEV. STEP	MP	PENRYN ULV CPU(2/3)	PART NO.	
APPROVAL	KK.BIN	REV	1.0	July 31, 2009 07:39:21 AM	BA41-0XXXXA	
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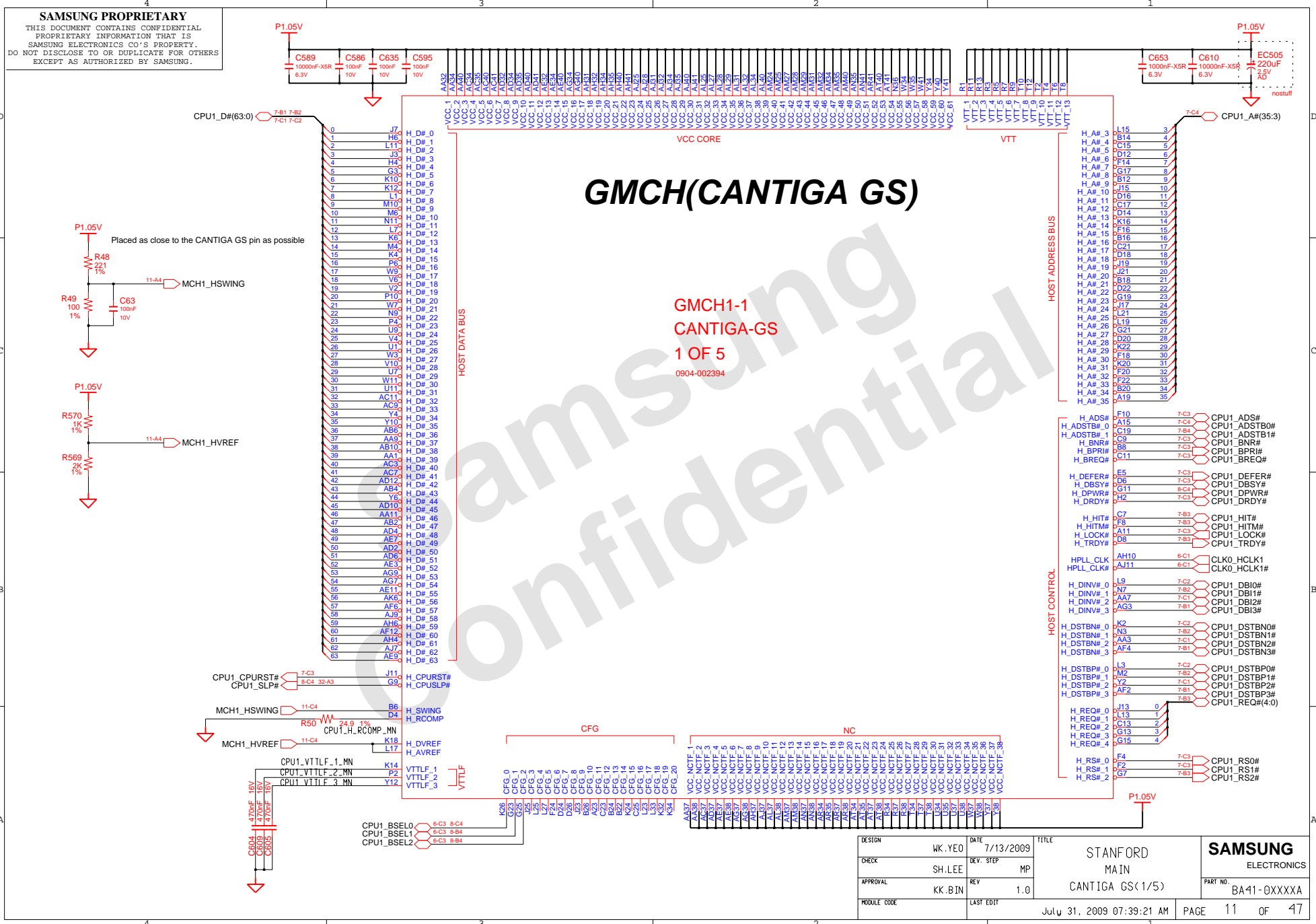
THERMAL SENSOR & FAN CONTROL



DESIGN	WK.YEO	DATE	7/13/2009	TITLE	STANFORD MAIN THERMAL MONITOR	SAMSUNG ELECTRONICS
CHECK	SH.LEE	DEV. STEP	MP			PART NO. BA41-0XXXXA
APPROVAL	KK.BIN	REV	1.0			
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A5		AP42		AR3		E19		E21		Y42	
A7	VSS 1	VSS 132	AP44	AR15	VSS 133	VSS 264	E17	E23	VSS 265	VSS 395	Y43
A9	VSS 2	VSS 133	AP8	AR17	VSS 134	VSS 265	E15	E25	VSS 266	VSS 394	Y36
A11	VSS 3	VSS 134	AP5	AR19	VSS 135	VSS 266	E9	E27	VSS 267	VSS 393	Y34
A15	VSS 4	VSS 129	AN39	AR21	VSS 136	VSS 261	E3	E29	VSS 268	VSS 392	Y12
A17	VSS 5	VSS 128	AN31	AR23	VSS 137	VSS 260	E1	E31	VSS 269	VSS 391	Y10
A19	VSS 6	VSS 127	AN29	AR25	VSS 138	VSS 259	D44	E39	VSS 270	VSS 390	V8
A21	VSS 7	VSS 126	AN27	AR27	VSS 140	VSS 257	D42	F6	VSS 272	VSS 388	V6
A23	VSS 8	VSS 125	AN25	AR29	VSS 141	VSS 256	D38	F42	VSS 273	VSS 387	W39
A25	VSS 9	VSS 124	AN23	AR31	VSS 142	VSS 255	D36	F44	VSS 274	VSS 386	W29
A27	VSS 10	VSS 123	AN21	AR35	VSS 143	VSS 254	D2	G1	VSS 275	VSS 385	W27
A29	VSS 11	VSS 122	AN19	AR37	VSS 144	VSS 253	C39	G3	VSS 276	VSS 384	W25
A31	VSS 12	VSS 121	AN17	AR39	VSS 145	VSS 252	C31	G9	VSS 277	VSS 383	W23
A39	VSS 13	VSS 120	AN15	AT6	VSS 146	VSS 251	C29	G15	VSS 278	VSS 382	W21
A41	VSS 14	VSS 119	AN3	AT9	VSS 147	VSS 250	C17	G11	VSS 279	VSS 381	W19
AA3	VSS 15	VSS 118	AM42	AT10	VSS 148	VSS 249	C25	G19	VSS 280	VSS 380	W17
AA5	VSS 16	VSS 117	AM38	AT12	VSS 149	VSS 248	C23	G21	VSS 281	VSS 379	W15
AA17	VSS 17	VSS 116	AM34	AT36	VSS 150	VSS 247	C21	G23	VSS 282	VSS 378	W13
AA19	VSS 18	VSS 115	AM30	AT39	VSS 151	VSS 246	C19	G25	VSS 283	VSS 377	W11
AA21	VSS 19	VSS 114	AM12	AT42	VSS 152	VSS 245	C17	G27	VSS 284	VSS 376	W9
AA23	VSS 20	VSS 113	AM10	AU3	VSS 153	VSS 244	C15	G29	VSS 285	VSS 375	W7
AA25	VSS 21	VSS 112	AM8	AU7	VSS 154	VSS 243	C11	G31	VSS 286	VSS 374	W5
AA27	VSS 22	VSS 111	AM6	AU9	VSS 155	VSS 242	C7	G37	VSS 287	VSS 373	W39
AA29	VSS 23	VSS 110	AL39	AU19	VSS 156	VSS 241	BD40	H6	VSS 288	VSS 372	W31
AA31	VSS 24	VSS 109	AL31	AU17	VSS 157	VSS 240	BD38	H10	VSS 289	VSS 371	W29
AA39	VSS 25	VSS 108	AL29	AU19	VSS 158	VSS 239	BD36	H34	VSS 290	VSS 370	W27
AB6	VSS 26	VSS 107	AL27	AU21	VSS 159	VSS 238	BD6	H38	VSS 291	VSS 369	W25
AB9	VSS 27	VSS 106	AL25	AT23	VSS 160	VSS 237	BD4	H42	VSS 292	VSS 368	W23
AB34	VSS 28	VSS 105	AL23	AT25	VSS 161	VSS 236	BD41	J3	VSS 293	VSS 367	W21
AB42	VSS 29	VSS 104	AL21	AU27	VSS 162	VSS 235	BD33	J15	VSS 294	VSS 366	W19
AC3	VSS 30	VSS 103	AL19	AU29	VSS 163	VSS 234	BD31	J17	VSS 295	VSS 365	W17
AC15	VSS 31	VSS 102	AL17	AU31	VSS 164	VSS 233	BD27	J19	VSS 296	VSS 364	W15
AC17	VSS 32	VSS 101	AL15	AU35	VSS 165	VSS 232	BD22	J21	VSS 297	VSS 363	W13
AC19	VSS 33	VSS 100	AL3	AU37	VSS 166	VSS 231	BD25	J23	VSS 298	VSS 362	W11
AC21	VSS 34	VSS 99	AK42	AU39	VSS 167	VSS 230	BD21	J25	VSS 299	VSS 361	W9
AC23	VSS 35	VSS 98	AK34	AV6	VSS 168	VSS 229	BD21	J27	VSS 300	VSS 360	T42
AC25	VSS 36	VSS 97	AK29	AT12	VSS 169	VSS 228	BD19	J29	VSS 301	VSS 359	T38
AC27	VSS 37	VSS 96	AK6	AV4	VSS 170	VSS 227	BD17	J31	VSS 302	VSS 358	T34
AC29	VSS 38	VSS 95	AJ39	AV36	VSS 171	VSS 226	BD15	J39	VSS 303	VSS 357	T32
AC31	VSS 40	VSS 93	AJ31	AV42	VSS 172	VSS 225	BD11	K6	VSS 304	VSS 356	T12
AC39	VSS 41	VSS 92	AJ29	AV44	VSS 173	VSS 224	BD9	K8	VSS 305	VSS 355	T10
AD9	VSS 42	VSS 91	AJ27	AW1	VSS 174	VSS 223	BD42	K34	VSS 306	VSS 354	T8
AD10	VSS 43	VSS 90	AJ25	AW3	VSS 175	VSS 222	BD42	K42	VSS 307	VSS 353	T6
AD12	VSS 44	VSS 89	AJ23	AW9	VSS 176	VSS 221	BD36	L3	VSS 308	VSS 352	R39
AD14	VSS 45	VSS 88	AJ21	AW11	VSS 177	VSS 220	BD12	L15	VSS 309	VSS 351	R31
AD34	VSS 46	VSS 87	AJ19	AW13	VSS 178	VSS 219	BD7	L17	VSS 310	VSS 350	R29
AD36	VSS 47	VSS 86	AJ17	AW15	VSS 179	VSS 218	BD7	L19	VSS 311	VSS 349	R27
AD38	VSS 48	VSS 85	AJ15	AW17	VSS 180	VSS 217	BA43	L21	VSS 312	VSS 348	R25
AD42	VSS 49	VSS 84	AJ13	AW19	VSS 181	VSS 216	BA39	L23	VSS 313	VSS 347	R23
AE3	VSS 50	VSS 83	AH42	AW21	VSS 182	VSS 215	BA33	L25	VSS 314	VSS 346	R21
AE15	VSS 51	VSS 82	AH38	AT23	VSS 183	VSS 214	BA31	L27	VSS 315	VSS 345	R19
AE17	VSS 52	VSS 81	AH36	AT25	VSS 184	VSS 213	BA29	L29	VSS 316	VSS 344	R17
AE19	VSS 53	VSS 80	AH34	AT27	VSS 185	VSS 212	BA27	L31	VSS 317	VSS 343	R15
AE21	VSS 54	VSS 79	AH12	AW29	VSS 186	VSS 211	BA25	L39	VSS 318	VSS 342	R13
AE23	VSS 55	VSS 78	AH10	AW31	VSS 187	VSS 210	BA23	M6	VSS 319	VSS 341	P42
AE25	VSS 56	VSS 77	AH8	AW33	VSS 188	VSS 209	BA21	M8	VSS 320	VSS 340	P34
AE27	VSS 57	VSS 76	AG39	AW35	VSS 189	VSS 208	BA19	M10	VSS 321	VSS 339	P8
AE29	VSS 58	VSS 75	AG37	AW37	VSS 190	VSS 207	BA17	M12	VSS 322	VSS 338	P6
AE31	VSS 59	VSS 74	AG31	AW39	VSS 191	VSS 206	BA15	M34	VSS 323	VSS 337	N39
AE39	VSS 60	VSS 73	AG29	AW42	VSS 192	VSS 205	BA13	M36	VSS 324	VSS 336	N29
AF3	VSS 61	VSS 72	AG27	AY27	VSS 193	VSS 204	BA9	M42	VSS 325	VSS 335	N27
AF8	VSS 62	VSS 71	AG25	AY34	VSS 194	VSS 203	BA9	N3	VSS 326	VSS 334	N25
AF34	VSS 63	VSS 70	AG23	AY42	VSS 195	VSS 202	BA3	N3	VSS 327	VSS 333	N23
AF42	VSS 64	VSS 69	AG21	AY44	VSS 196	VSS 201	BA1	N15	VSS 328	VSS 332	N21
AG3	VSS 65	VSS 68	AG19	BA	VSS 197	VSS 200	BA3	N17	VSS 329	VSS 331	N19
AG15	VSS 66	VSS 67	AG17	B6	VSS 198	VSS 199	B36	N19	VSS 330		

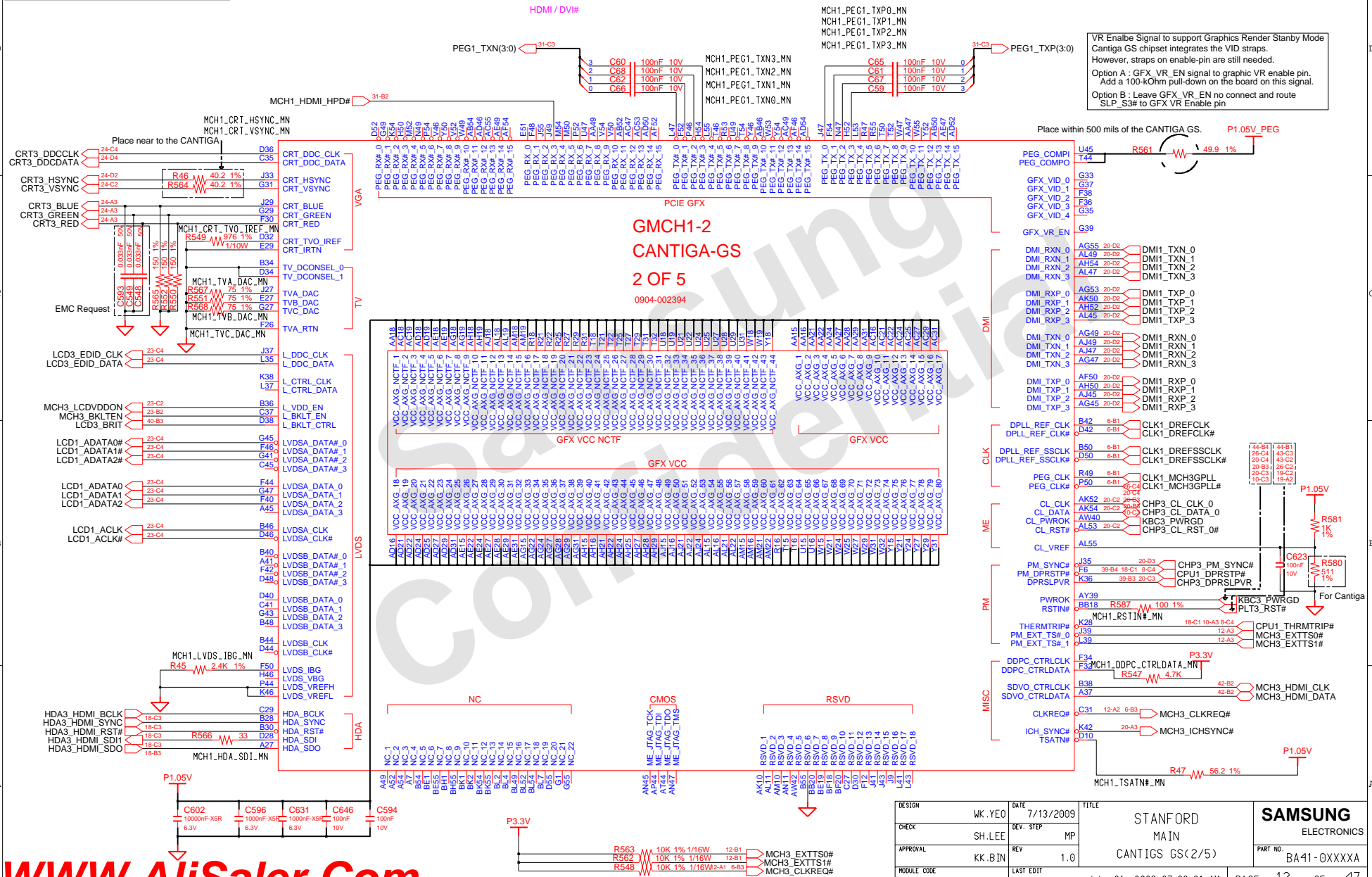
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GMCH(CANTIGA GS)





SM_DRAMRST#	Leave as NC in DDR2 mode. Used only in DDR3 mode.
SM_PWROK	Connect to GND in DDR2 mode

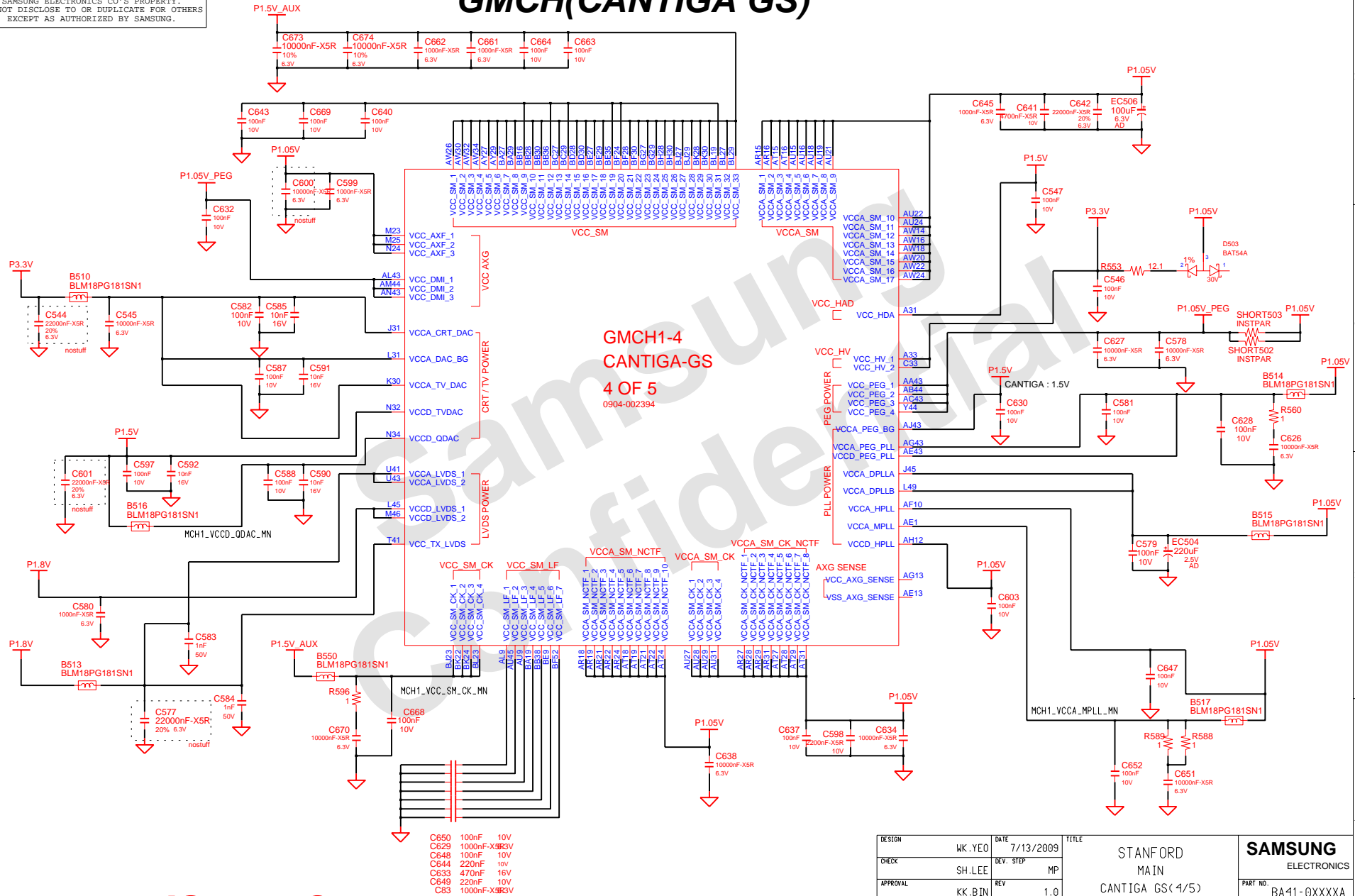
GMCH(CANTIGA GS)

GMCH1-3
CANTIGA-GS
3 OF 5

0904-00239

DESIGN	WK.YEO	DATE	7/13/2009	TITLE STANFORD MAIN CANTIGS GS(3/5)			
CHECK	SH.LEE	REV. STEP	MP				
APPROVAL	KK.BIN	REV	1.0		PART NO. BA41-0XXXXA		
MODULE CODE	LAST EDIT		July 31, 2009 07:39:21 AM		PAGE	13 OF 47	

GMCH(CANTIGA GS)

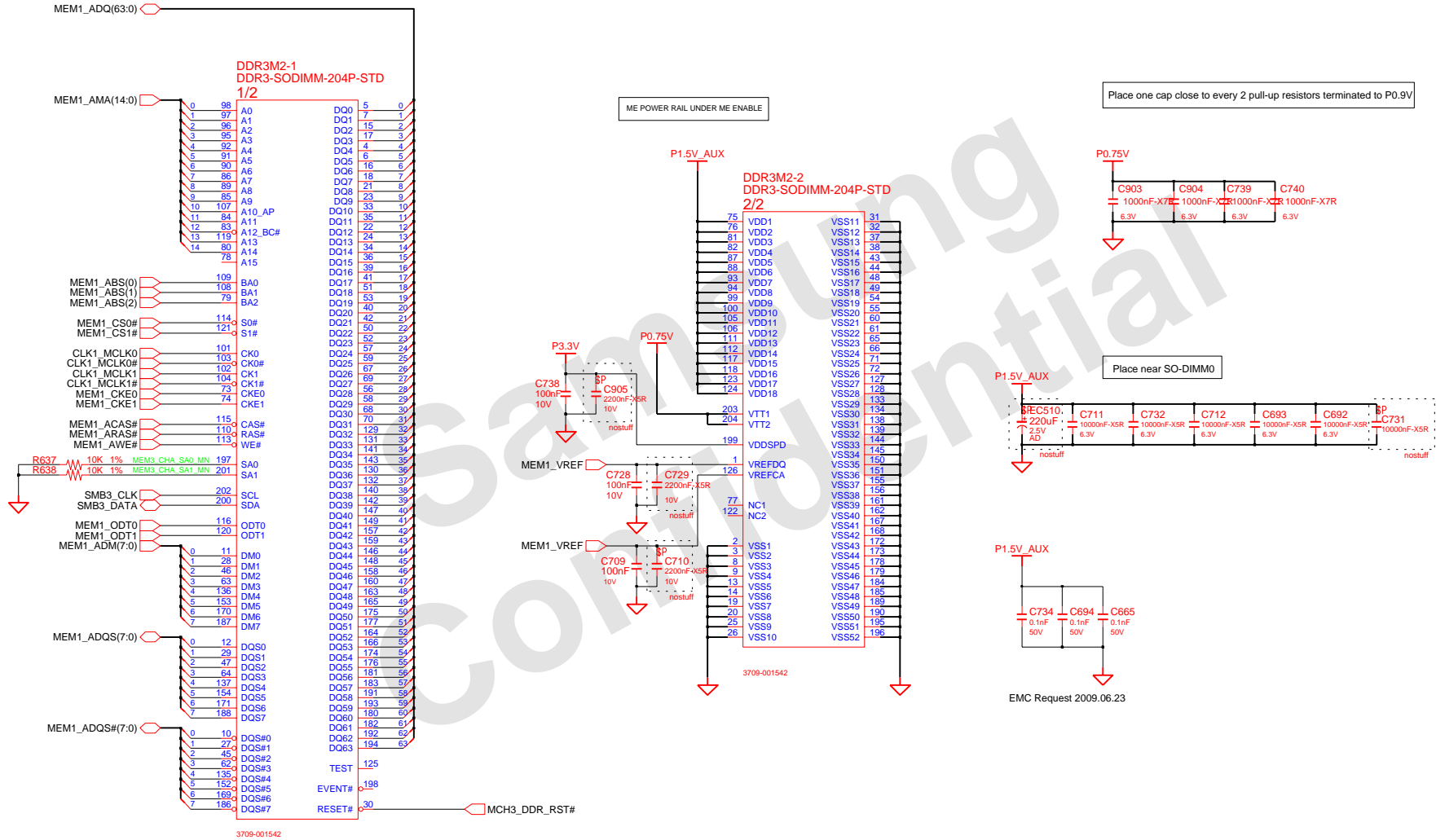


VSS

DESIGN	WK.YEO	DATE	7/13/2009	TITLE			STANFORD MAIN			SAMSUNG ELECTRONICS		
CHECK	SH.LEE	DEV. STEP	MP									
APPROVAL	KK.BIN	REV	1.0	CANTIGS GS(5/5)			PART NO.			BA41-0XXXXA		
MODULE CODE		LAST EDIT					July 31, 2009 07:39:21 AM			PAGE	15	OF

DDR SO-DIMM #0

Height : 5.2mm (Standard)



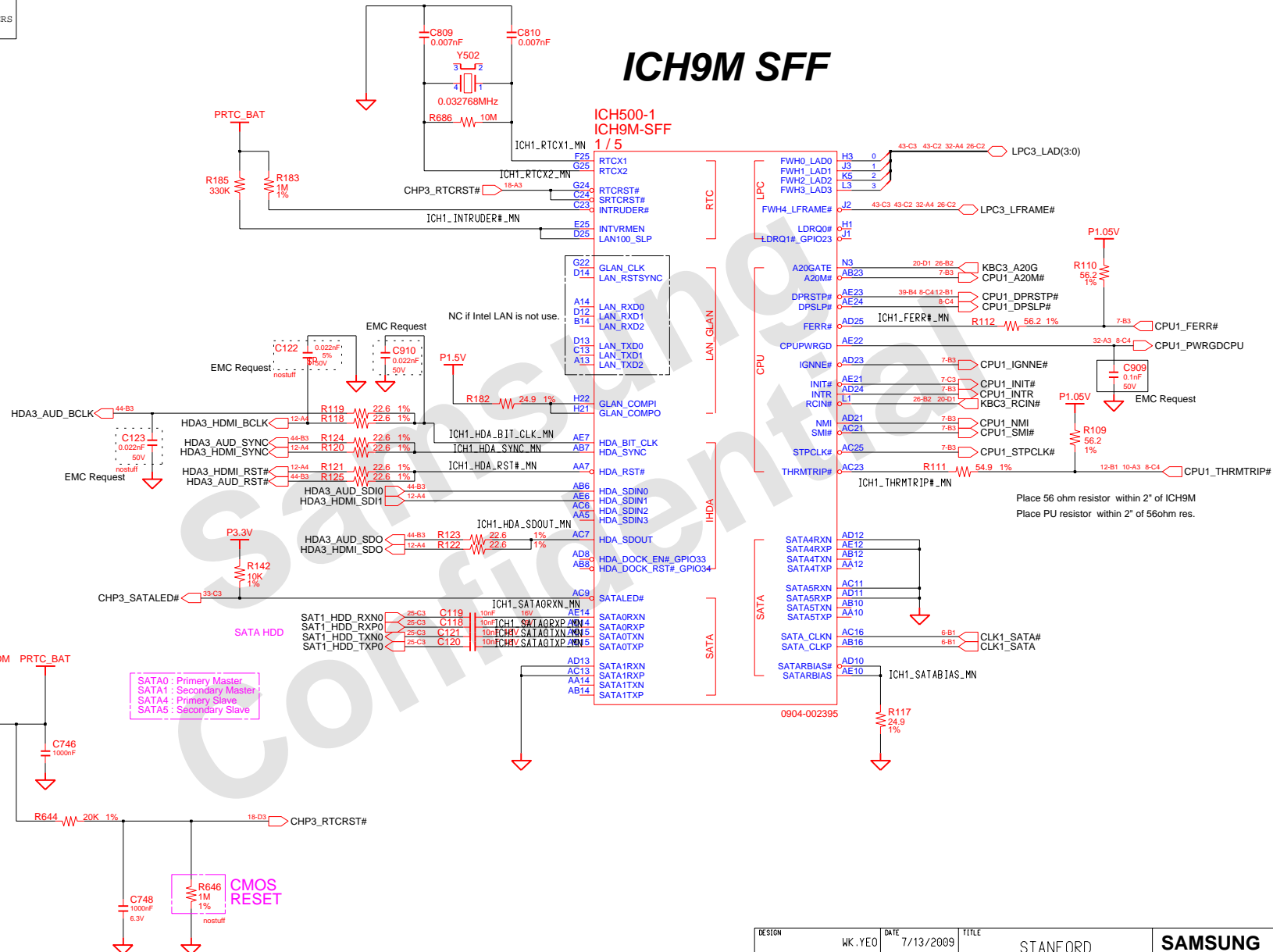
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CHECK	SH.LEE	DEV. STEP	MP		DDR3 SODIMM CH.0	
APPROVAL	KK.BIN	REV	1.0			
MODULE CODE		LAST EDIT	July 31, 2009 07:39:21 AM	PAGE	16 OF 47	

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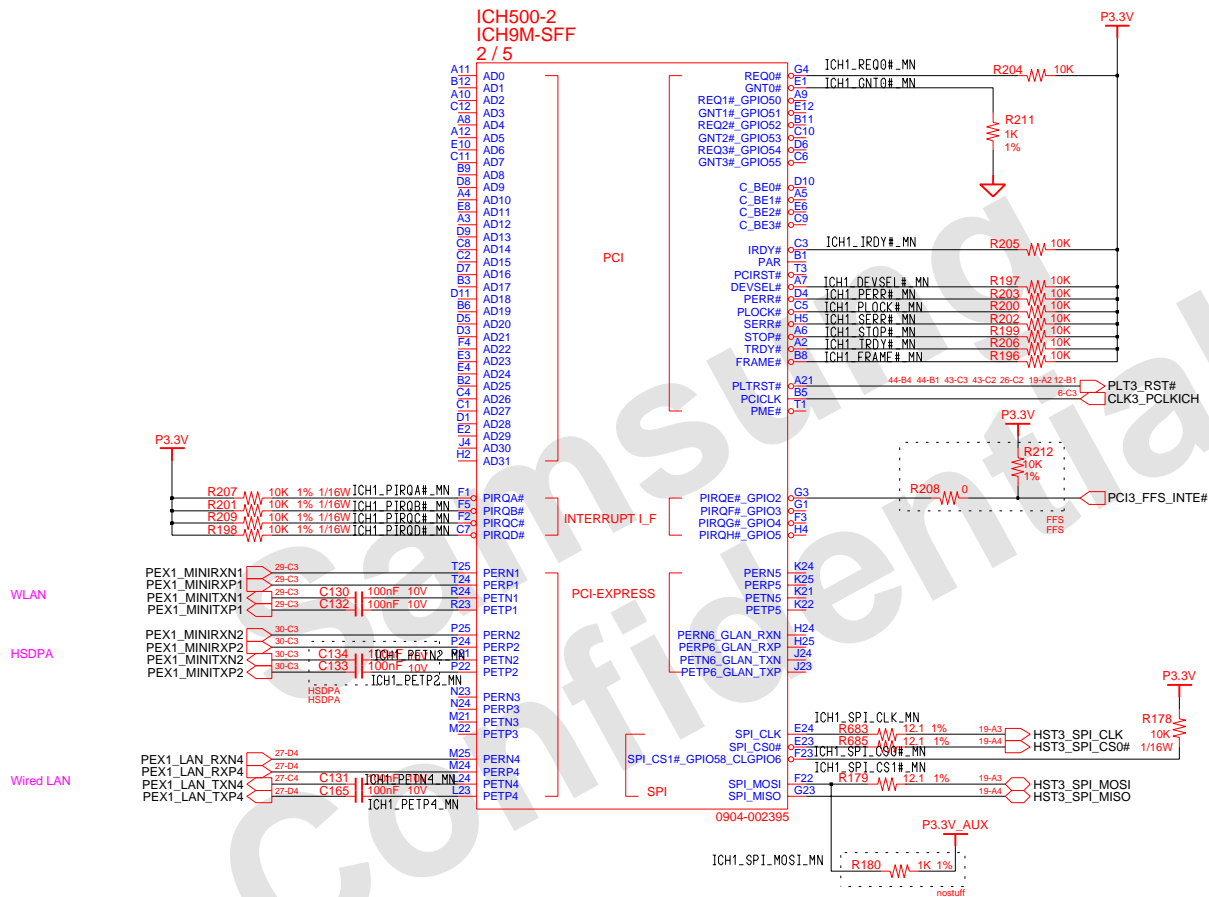
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ICH9M SFF

ICH500-1
 ICH9M-SFF
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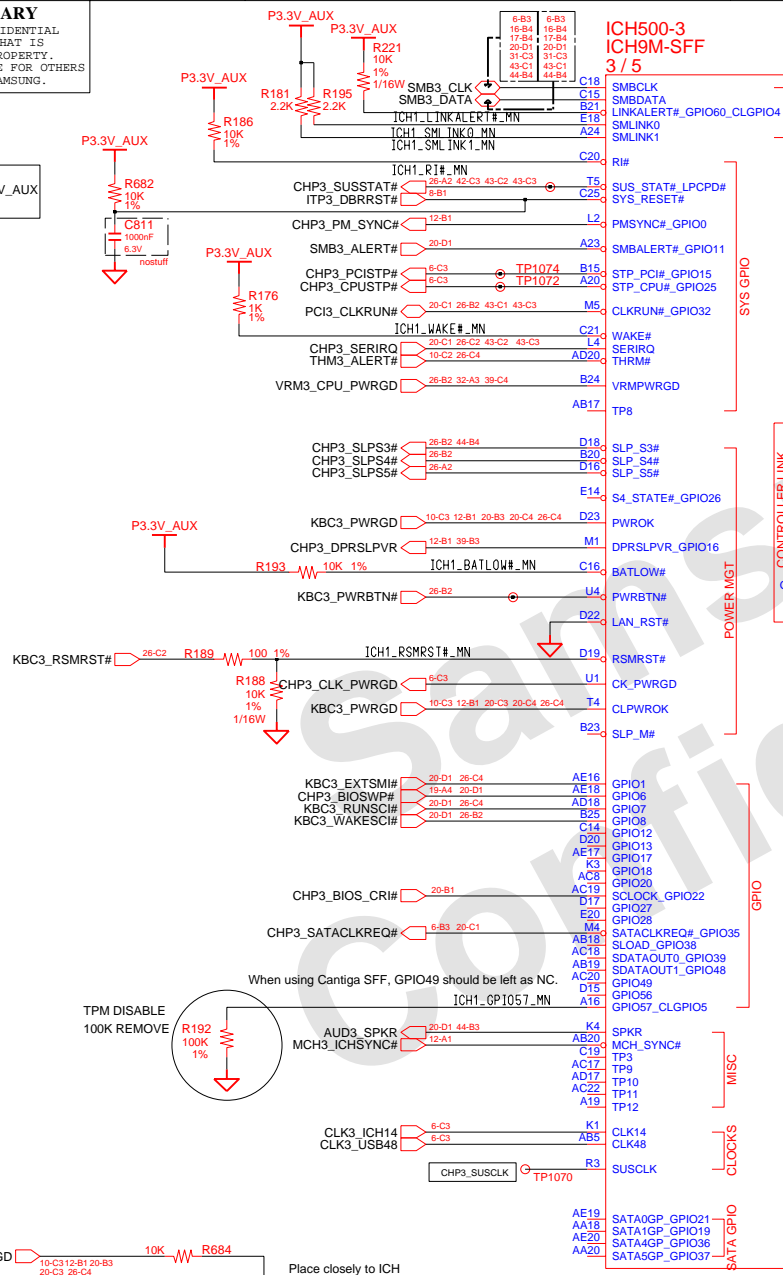


ICH500-2
ICH9M-SFF
2 / 5



BIOS	PCI3_GNT0#	SPI3_CS1#
LPC	HIGH	HIGH
SPI	LOW	HIGH
PCI	HIGH	LOW

DESIGN	WK.YEO	DATE	7/13/2009	<div>STANFORD MAIN</div> <div>ICH9M SFF(2/5)</div>	<div>SAMSUNG</div> <div>ELECTRONICS</div>	
CHECK	SH.LEE	DEV. STEP	MP			
APPROVAL	KK.BIN	REV	1.0		PART NO.	BA41-0XXXXA
MODULE CODE	LAST EDIT		July 31, 2009 07:39:21 AM		PAGE	19 OF 47



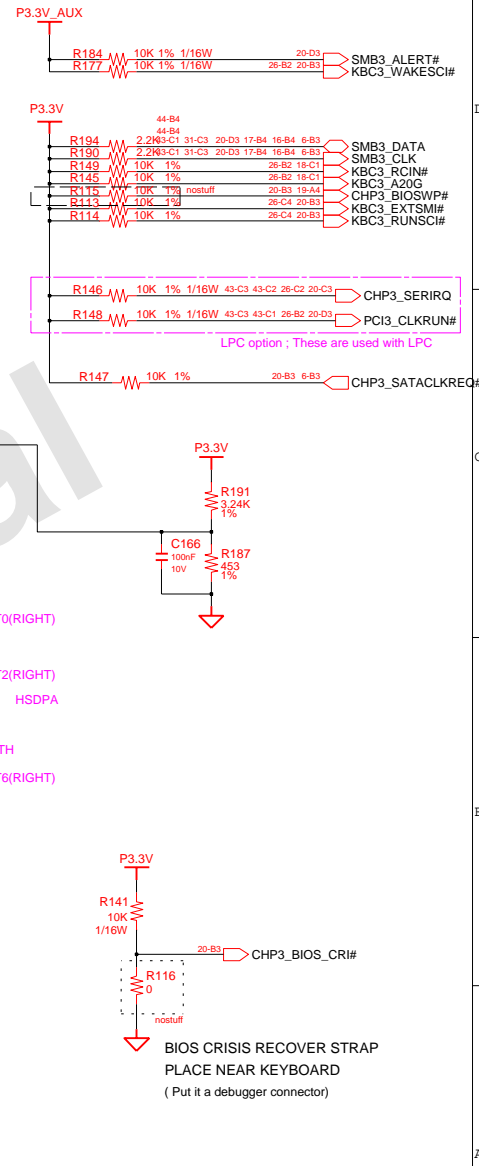
SMB

DM10RXN	V25	12C1	DM11_RXN_0
DM10RXN	V24	12C1	DM11_RXP_0
DM10TXN	U34	12C1	DM11_TXN_0
DM10TXN	U23	12C1	DM11_TXP_0

DIRECT MEDIA INTERFACE

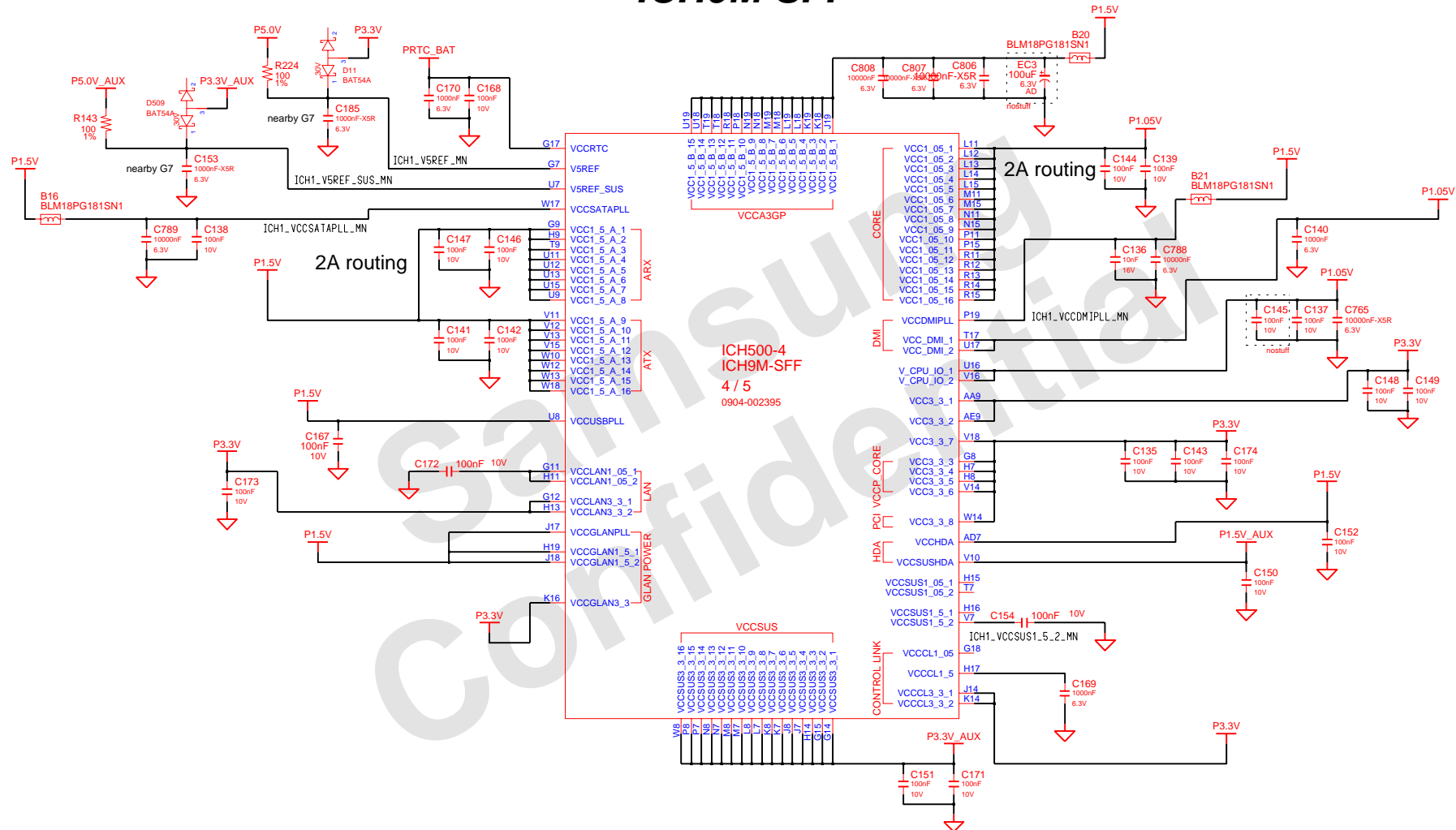
DM11RXN	W23	12C1	DM11_RXN_1
DM11RXP	W24	12C1	DM11_RXP_1
DM11TXN	V21	12C1	DM11_TXN_1
DM11TXP	V22	12C1	DM11_TXP_1
DM12RXN	Y24	12C1	DM11_RXN_2
DM12RXP	Y25	12C1	DM11_RXP_2
DM12TXN	Y21	12C1	DM11_TXN_2
DM12TXP	Y22	12C1	DM11_TXP_2
DM13RXN	AB24	12C1	DM11_RXN_3
DM13RXP	AB25	12C1	DM11_RXP_3
DM13TXN	AB22	12C1	DM11_TXN_3
DM13TXP	A24	12C1	DM11_TXP_3
DM1_CLKN	T22	6-B1	CLK1_P_CIEICH#
DM1_CLKP	T22	6-B1	CLK1_P_CIEICH
DM1_ZCOMP	AB21		P15+
DM1_IRCOMP	AB22		

R140 24.9 1%



DESIGN	WK.YE0	DATE	7/13/2009	TITLE STANFORD MAIN ICH9M SFF(3/5)	SAMSUNG ELECTRONICS		
CHECK	SH.LEE	DEV. STEP	MP				
APPROVAL	KK.BIN	REV	1.0			PART NO.	BA41-0XXXXA
MODULE CODE	LAST EDIT					July 31, 2009 07:39:21 AM	PAGE 20 OF 47

ICH9M SFF



DESIGN	WK.YEO	DATE	7/13/2009	TITLE	STANFORD MAIN ICH9M SFF(4/5)	SAMSUNG ELECTRONICS
CHECK	SH.LEE	DEV. STEP	MP			PART NO. BA41-0XXXXA
APPROVAL	KK.BIN	REV	1.0			
MODULE CODE		LAST EDIT				
July 31, 2009 07:39:21 AM						PAGE 21 OF 47

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BIOS CODE

ICH9M SFF

02 VERIFY REAL MODE
03 DISABLE NMI
04 GET CPU TYPE
06 INIT. SYSTEM H/W
08 INIT. CHIPSET REG.
09 SET IN POST FLAG
0A INIT CPU.REG
0B CPU CACHE ON
0C INIT.CACHE TO POST
0E INIT. I/O VALUE
0F ENABLE THE L-BUS IDE
10 INIT. POWER MANAGER
11 LOAD ALTERNATE REG.
13 PCI BUS MASTER RESET
WITH INITIAL POST VALUE
14 INIT. KEYBOARD CONTROLLER
16 CHECK CHECKSUM
18 8254 TIMER INIT.
1A 8237 DMA CONTROLLER INIT.
1C RESET INTERRUPT CONTROLLER
20 TEST DRAM REFRESH
22 TEST 8742 KEYBOARD CONTROLLER
24 SET ES SEGMENT REG. TO 4GB
26 ENABLE A20
28 AUTO SIZING DRAM
32 COMPUTE THE CPU SPEED
34 TESET CMOS RAM
38 SHADOW SYSTEM BIOS ROM
3A AUTO SIZING CACHE
3C CONFIGURE ADVANCED CHIPSET REG.
3D LOAD ALTER REG. WITH CMOS VALUE
42 INIT. INTERRUPT VECTOR
44 INIT. BIOS INTERRUPT
46 CHECK ROM COPYRIGHT NOTICE
47 INIT. I20 SUPPORT IF INSTALLED
48 CHECK VIDEO CONFIGURE AGAINST CMOS
49 INIT. PCI BUS AND DEVICE
4A INIT. ALL VIDEO BIOS ROM
4C SHADOW VIDEO BIOS ROM
50 DISPLAY CPU TYPE AND SPEED
52 TEST KEYBOARD
54 SET KEYCLICK IF ENABLED
56 ENABLE KEYBOARD
58 TEST FOR UNEXPECTED INTERRUPTS
5A DISPLAY * PRESS SETUP*
5C TEST RAM BETWEEN 512K AND 640K
60 TEST EXTENDED MEMORY
62 TEST EXTENDED MEMORY ADDRESS LINE
64 JUMP TO USER PATCH 1

66 CONFIGURE ADVANCE CACHE REG.
6A DISPLAY EXTERNAL CACHE SIZE
6C DISPLAY SHADOW MESSAGE
6E DISPLAY NON-DISPOSABLE SEGMENT
70 DISPLAY ERROR MESSAGE
72 CHECK FOR CONFIGURATION ERROR
74 TEST REAL-TIME CLOCK
76 CHECK FOR KEYBOARD EERROR
7C SETUP HARDWARE INTERRUPT VECTOR
7E TEST COPROCESSER IF PRESENT
80 DISABLE ON-BOARD I/O PORT
82 DETECT AND INSTALL EXT.RS232C
84 DETECT AND INSTALL EXT.PARALLEL
86 RE-INIT. ON-BOARD I/O PORT
88 INIT. BIOS DATA ROM
8A INIT.EXTENDED BIOS DATA AREA
8C INIT. FDD CONTROLLER
9A SHADOW OPTION ROMS
9C SETUP POWER MANAGEMENT
9E ENABLE H/W INTERRUPT
A0 SET TIME OF DAY
A4 INIT. TYPEMATIC RATE
A8 ERASE F2 PROMPT
AA SCAN FOR F2 KEY STROKE
AC ENTER SETUP
AE CLEAR IN POST FLAG
B0 CHECK FOR ERRORS
B2 POST DONE-PREPARE TO BOOT O/S
B4 ONE BEEP
B6 CHECK PASSWORD (OPTION)
B7 ACPI INIT
BA DMI INIT
BE CLEAR SCREEN
C0 TRY BOOT WITH INT19
D0 INTERRUPT HANDLER ERROR
D2 UNKNOWN INTERRUPT ERROR
D4 PENDING INTERRUPT ERROR
D6 SHUTDOWN 5
D8 SHUTDOWN ERROR
DA EXTENDED BLOCK MOVE
DC SHUTDOWN 10
89 ENABLE NMI
90 INIT. HDD CONTROLLER
91 INIT. LOCAL BUS HDD CONTROLLER
92 JUMP TO USER PATCH 2
94 DISABLE A20 ADDRESS LINE
96 CLEAR HUGE ES SEGMENT REG.
98 SEARCH FOR OPTION ROMS

AA1	VSS. 1	VSS. 133	R9
AA11	VSS. 2	VSS. 134	T10
AA13	VSS. 3	VSS. 135	T11
AA15	VSS. 4	VSS. 136	T12
AA16	VSS. 5	VSS. 137	T13
AA17	VSS. 6	VSS. 138	T14
AA19	VSS. 7	VSS. 139	T15
AA21	VSS. 8	VSS. 140	T16
AA22	VSS. 9	VSS. 141	T2
AA25	VSS. 10	VSS. 142	T23
AA4	VSS. 11	VSS. 143	T8
AA6	VSS. 12	VSS. 144	U10
AA8	VSS. 13	VSS. 145	U14
AB11	VSS. 14	VSS. 146	U21
AB13	VSS. 15	VSS. 147	U22
AB15	VSS. 16	VSS. 148	U25
AB3	VSS. 17	VSS. 149	U5
AB9	VSS. 18	VSS. 150	V17
AC1	VSS. 19	VSS. 151	V19
AC10	VSS. 20	VSS. 152	V23
AC12	VSS. 21	VSS. 153	V3
AC14	VSS. 22	VSS. 154	V8
AC24	VSS. 23	VSS. 155	V9
AC4	VSS. 24	VSS. 156	W1
AD16	VSS. 25	VSS. 157	W14
AD19	VSS. 26	VSS. 158	W15
AD2	VSS. 27	VSS. 159	W16
AD22	VSS. 28	VSS. 160	W19
AD6	VSS. 29	VSS. 161	W21
AD9	VSS. 30	VSS. 162	W22
AE11	VSS. 31	VSS. 163	W25
AE13	VSS. 32	VSS. 164	W4
AE15	VSS. 33	VSS. 165	W5
AE3	VSS. 34	VSS. 166	W9
AE4	VSS. 35	VSS. 167	Y23
AE8	VSS. 36	VSS. 168	Y3
B10	VSS. 37		
B13	VSS. 38		
B16	VSS. 39		
B19	VSS. 40		
B22	VSS. 41		
B4	VSS. 42		
B7	VSS. 43		
D2	VSS. 44		
D24	VSS. 45		
E11	VSS. 46		
E13	VSS. 47		
E15	VSS. 48		
E17	VSS. 49		
E19	VSS. 50		
E21	VSS. 51		
E5	VSS. 52		
E7	VSS. 53		
E9	VSS. 54		
F24	VSS. 55		
G10	VSS. 56		
G13	VSS. 57		
G16	VSS. 58		
G19	VSS. 59		
G2	VSS. 60		
G21	VSS. 61		
G5	VSS. 62		
H10	VSS. 63		
H12	VSS. 64		
H18	VSS. 65		
H23	VSS. 66		
J0	VSS. 67		
J11	VSS. 68		
J12	VSS. 69		
J13	VSS. 70		
J15	VSS. 71		
J16	VSS. 72		
J21	VSS. 73		
J22	VSS. 74		
J25	VSS. 75		
J5	VSS. 76		
J9	VSS. 77		
K10	VSS. 78		
K11	VSS. 79		
K12	VSS. 80		
K13	VSS. 81		
K17	VSS. 82		
K2	VSS. 83		
K23	VSS. 84		
K3	VSS. 85		
K9	VSS. 86		
L16	VSS. 87		
L17	VSS. 88		
L21	VSS. 89		
L22	VSS. 90		
L23	VSS. 91		
L5	VSS. 92		
L9	VSS. 93		
M10	VSS. 94		
M13	VSS. 95		
M14	VSS. 96		
M16	VSS. 97		
M3	VSS. 98		
M4	VSS. 99		
M6	VSS. 100		
N10	VSS. 101		
N12	VSS. 102		
N13	VSS. 103		
N14	VSS. 104		
N15	VSS. 105		
N16	VSS. 106		
N17	VSS. 107		
N18	VSS. 108		
N19	VSS. 109		
N2	VSS. 110		
N23	VSS. 111		
N25	VSS. 112		
N3	VSS. 113		
N4	VSS. 114		
N5	VSS. 115		
N6	VSS. 116		
N7	VSS. 117		
N8	VSS. 118		
N9	VSS. 119		
P1	VSS. 120		
P17	VSS. 121		
P23	VSS. 122		
P3	VSS. 123		
P11	VSS. 124		
P18	VSS. 125		
P19	VSS. 126		
P2	VSS. 127		
P25	VSS. 128		
P26	VSS. 129		
P27	VSS. 130		
P5	VSS. 131		
P6	VSS. 132		

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ICH9M-SFF

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GND

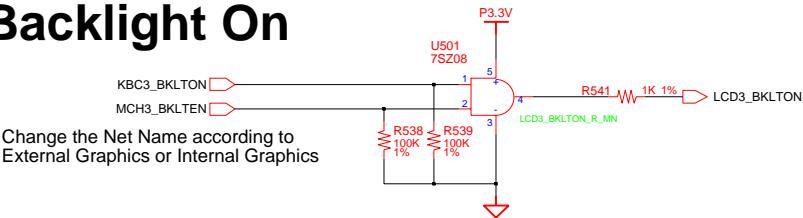
0904-002395

VSS_NCTF_1
VSS_NCTF_2
VSS_NCTF_3
VSS_NCTF_4

DESIGN	WK.YEO	DATE	7/13/2009	TITLE	STANFORD MAIN	SAMSUNG ELECTRONICS
CHECK	SH.LEE	DEV. STEP	MP			
APPROVAL	KK.BIN	REV	1.0		ICH9M SFF(5/5)	PART NO. BA41-0XXXXA
MODULE CODE		LAST EDIT		July 31, 2009 07:39:21 AM	PAGE 22	OF 47

LVDS

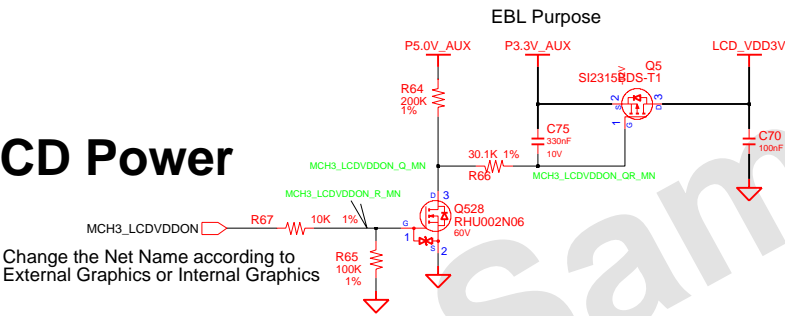
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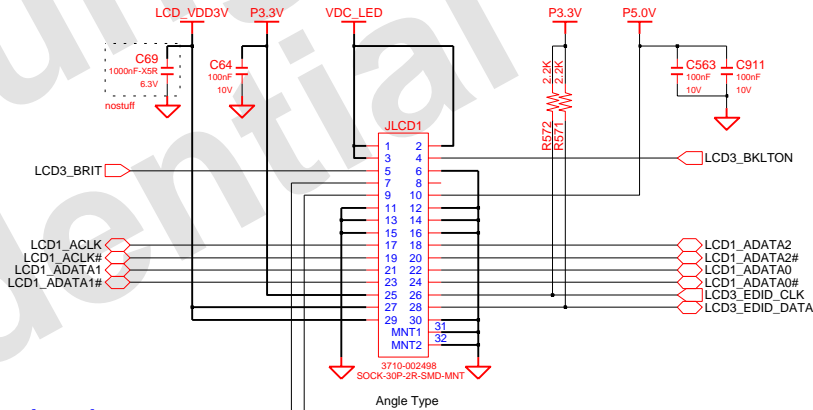
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External Graphics or Internal Graphics

1Ch. LCD Connector + CAMERA

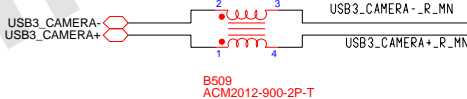
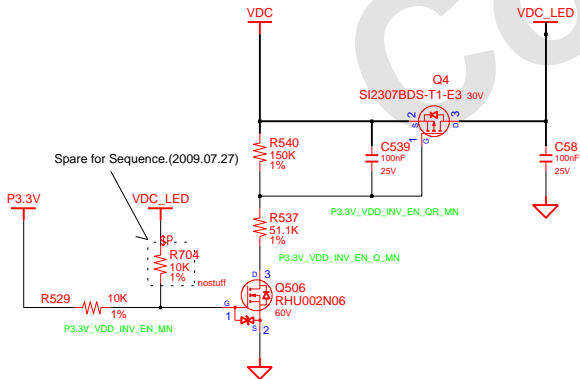
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Change the Net Name according to
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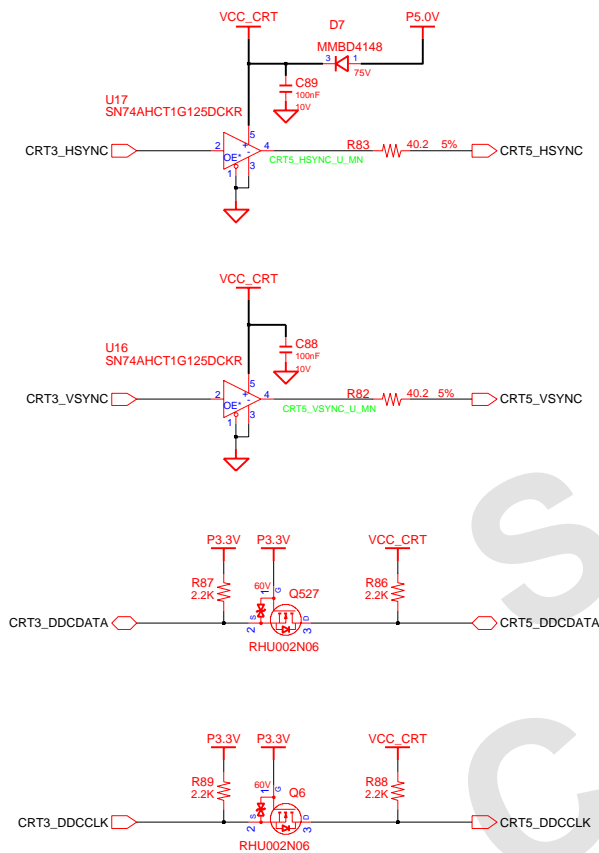


Inverter Power

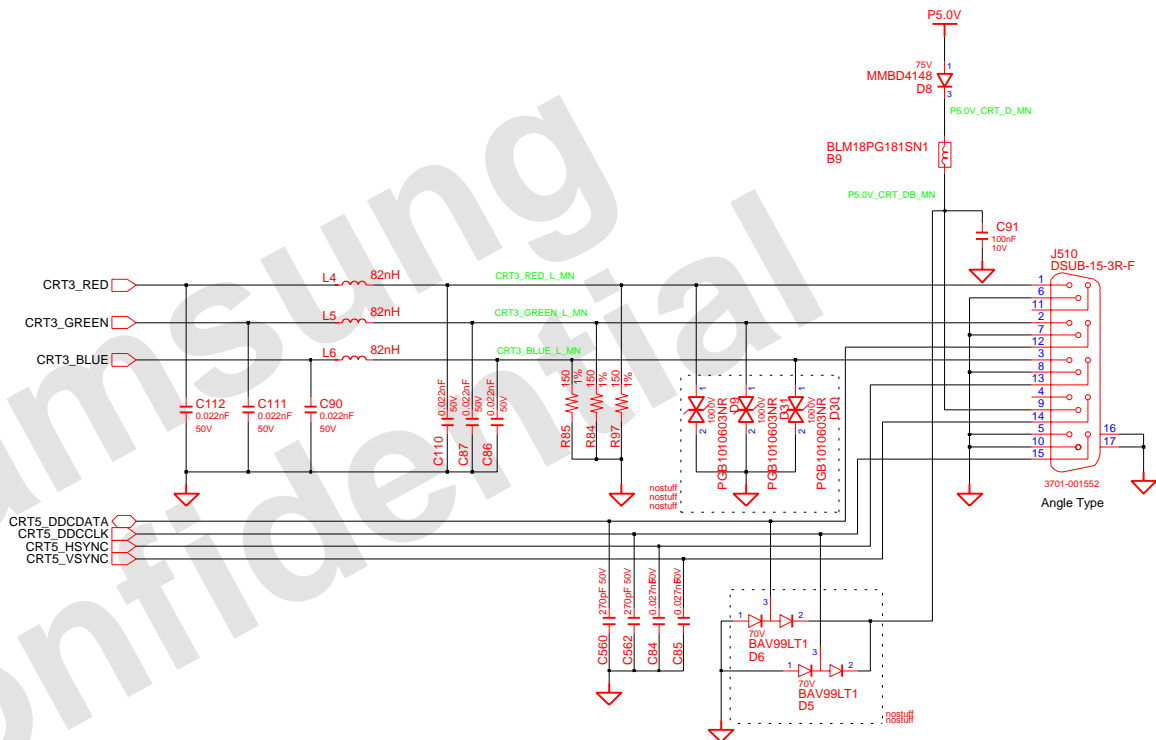



DESIGN	WK.YEO	DATE	7/13/2009	TITLE	STANFORD MAIN LED LCD I/F	SAMSUNG ELECTRONICS
CHECK	SH.LEE	DEV. STEP	MP			PART NO. BA41-0XXXXA
APPROVAL	KK.BIN	REV	1.0			
MODULE CODE		LAST EDIT	July 31, 2009 07:39:21 AM	PAGE	23	OF 47

CRT

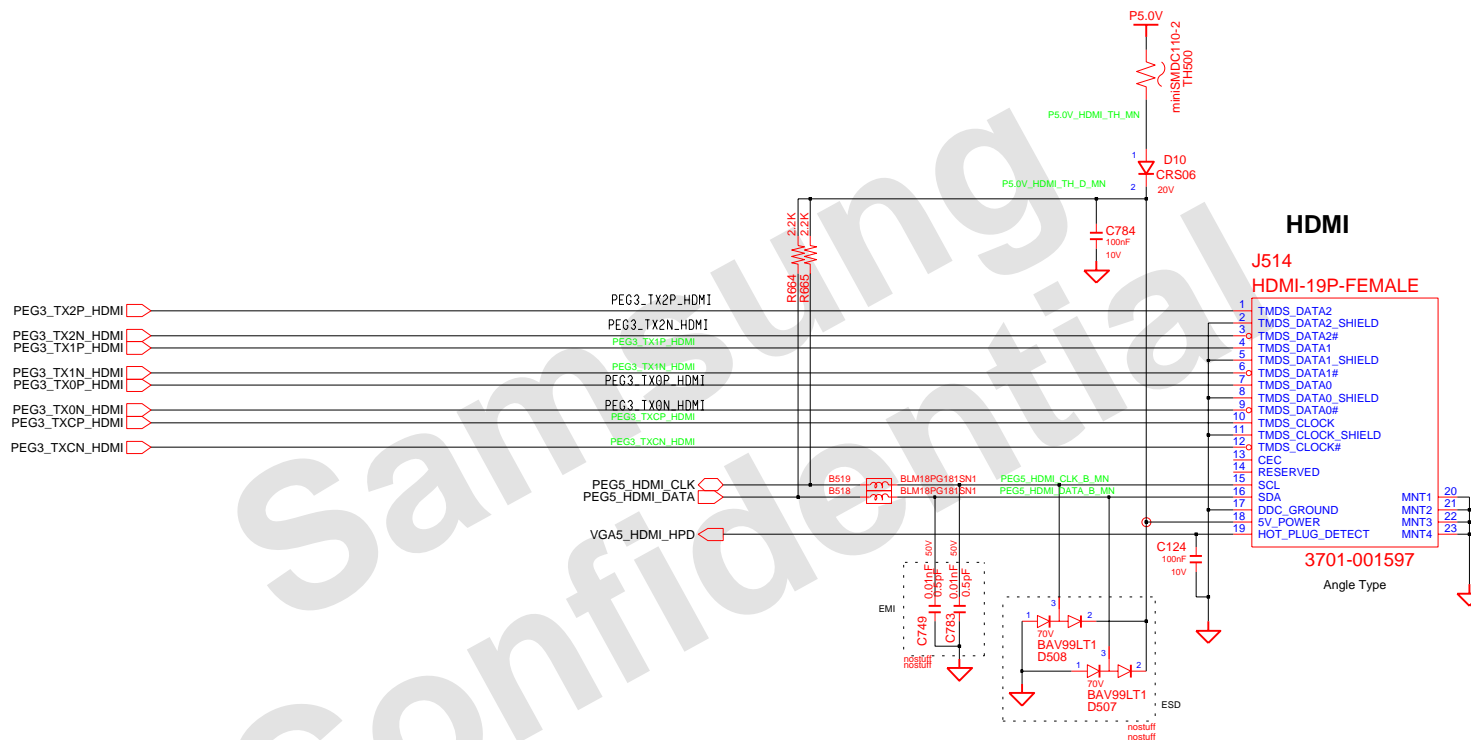


Check "CRT3_DDCCLK/DATA" Voltage Level
2N06 Can be replaced with SM6K2



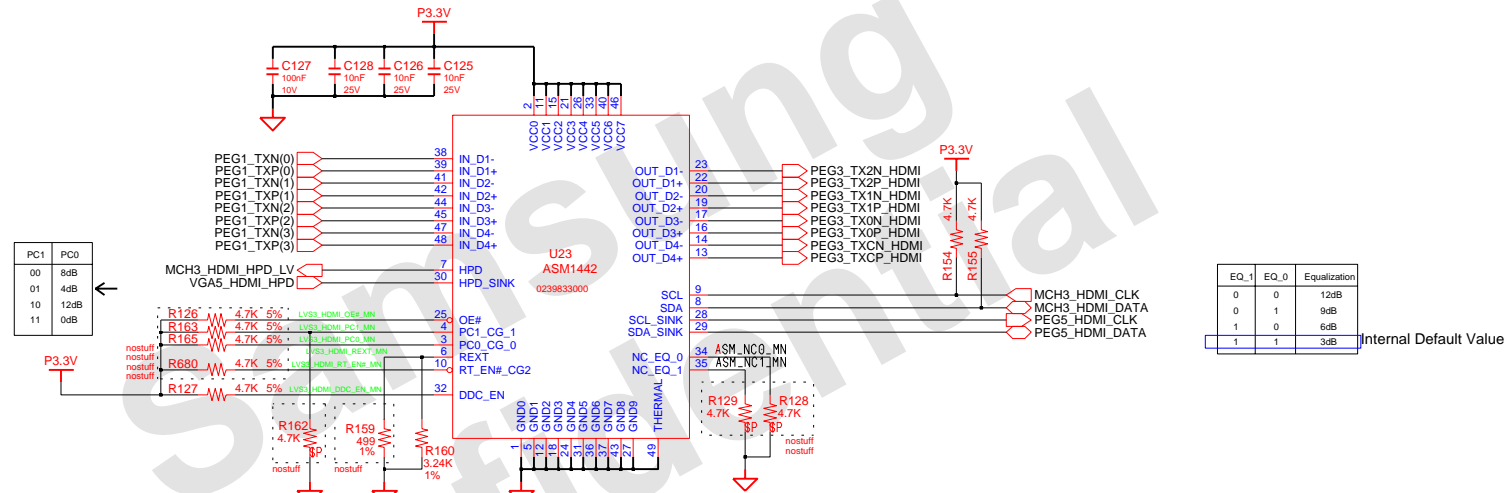
DESIGN	WK.YE0	DATE	7/13/2009	STANFORD MAIN CRT I/F			
CHECK	SH.LEE	DEV. STEP	MP				
APPROVAL	KK.BIN	REV	1.0			PART NO.	BA41-0XXXXA
MODULE CODE	LAST EDIT		July 31, 2009 07:39:21 AM			PAGE	24 OF 47

HDMI

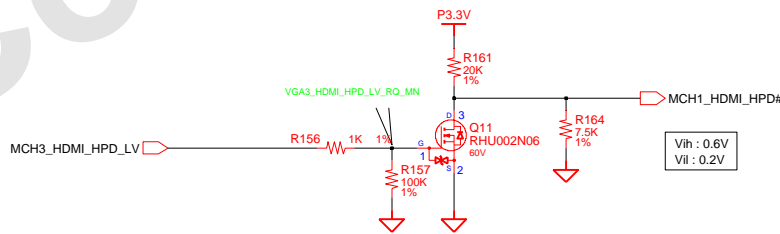


DESIGN	WK.YEO	DATE	7/13/2009	STANFORD MAIN HDMI I/F	SAMSUNG ELECTRONICS	
CHECK	SH.LEE	DEV. STEP	MP			
APPROVAL	KK.BIN	REV	1.0			
MODULE CODE		LAST EDIT				
					PART NO.	BA41-0XXXXA

HDMI Level Shifter for Int. Graphic only

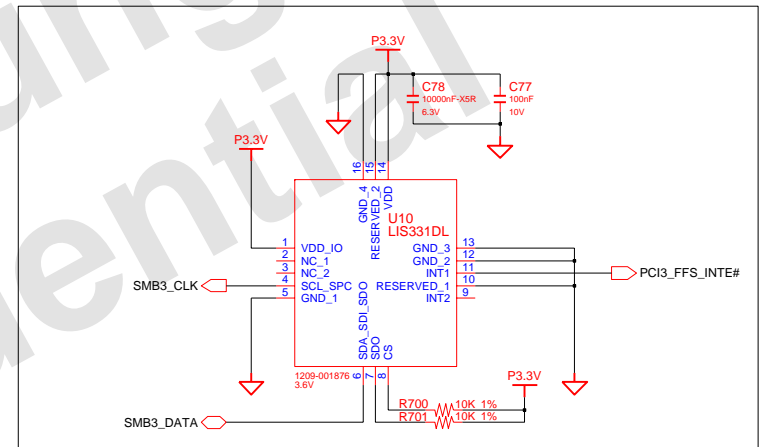
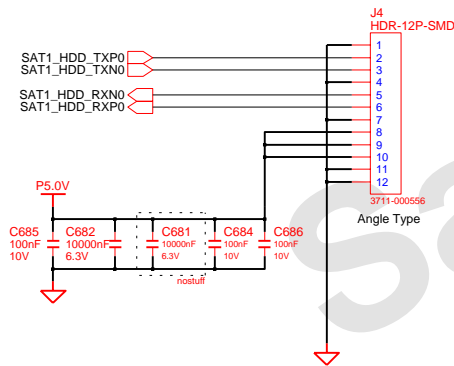


CG_2	CG_1	CG_0	Swing	Pre-amp	Slew rate
0	0	0	450mV	0dB	0dB
0	0	1	490mV	0dB	-3dB
0	1	0	450mV	0dB	-3dB
0	1	1	460mV	0dB	-4dB
1	0	0	340mV	0dB	0dB
1	0	1	400mV	2dB	0dB
1	1	0	400mV	2dB	0dB
1	1	1	420mV	0dB	0dB



HDMI Level Shifter	REXT(Pin6)	PC1_CG0(Pin3)	PC1_CG1(Pin4)	RT_EN#_CG2(Pin10)	NC_EQ_0(Pin34)	NC_EQ_1(Pin35)	Note
PS8101	499 phm	stuff	nostuff	nostuff	NC	NC	
ASM1442	3.4K(3.24~3.3K)	nostuff	nostuff	nostuff	nostuff	nostuff	Internal PUPD exist CGs nostuff is 450mV swing

DESIGN	WK.YEO	DATE	7/13/2009	TITLE	STANFORD MAIN HDMI LEVEL SHIFTER	SAMSUNG ELECTRONICS
CHECK	SH.LEE	DEV. STEP	MP			PART NO. BA41-0XXXXA
APPROVAL	KK.BIN	REV	1.0			
MODULE CODE		LAST EDIT	July 31, 2009 07:39:21 AM	PAGE	26	OF 47



FFS
FFS
FFS
FFS
FFS

DESIGN	WK.YE0	DATE	7/13/2009	TITLE		STANFORD MAIN		SAMSUNG ELECTRONICS	
CHECK	SH.LEE	DEV. STEP	MP						
APPROVAL	KK.BIN	REV	1.0	SATA HDD I/F & FFS		PART NO.		BA1-0XXXXA	
MODULE CODE		LAST EDIT				July 31, 2009 07:39:21 AM		PAGE	27

3.3V MICOM

3.3V MICOM

3.3V MICOM

MICOM_VCC0_R_MN

C706 100nF 10V

C727 100nF 10V

C708 100nF 10V

C726 100nF 10V

VCC0

VCC1

VCC2

AVCC

U511 MEC1308-NU

BA09-00021A

NRESET_OUT GPIO06

GPIO07_PWM3

GPIO08_RXD

GPIO09_TXD

OUT0_SCI

OUT1

OUT7_NSMI

OUT8_KBRST

OUT9_PWM2

OUT10_PWM0

PWM1_OUT11

124

125

123

122

121

120

118

KBC3_L

KBC3_E

KBC3_R

KBC3_W

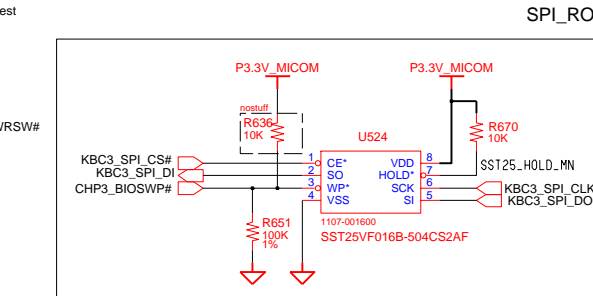
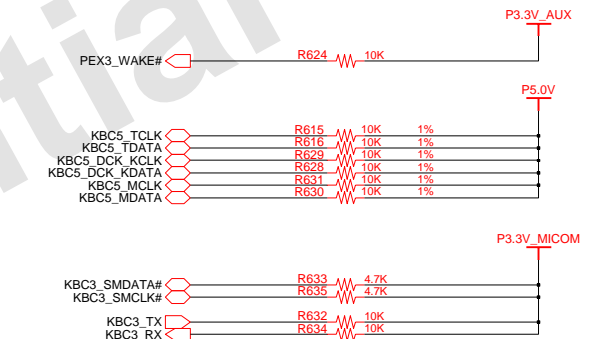
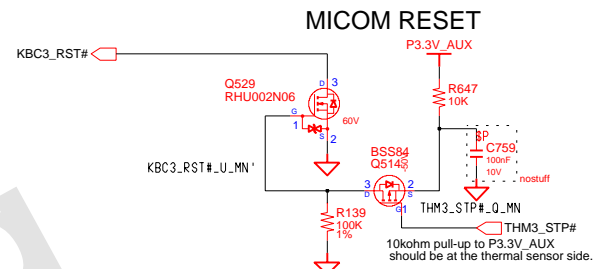
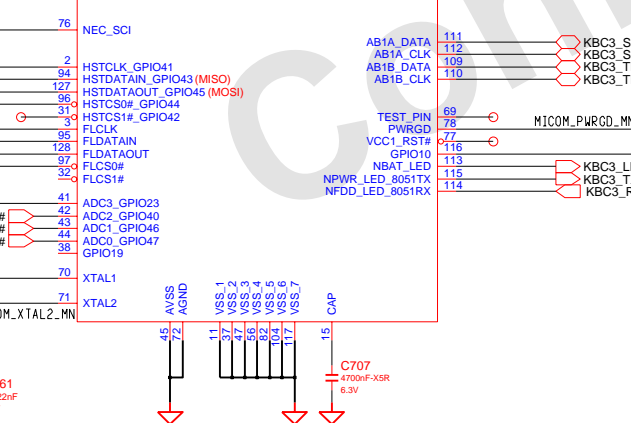
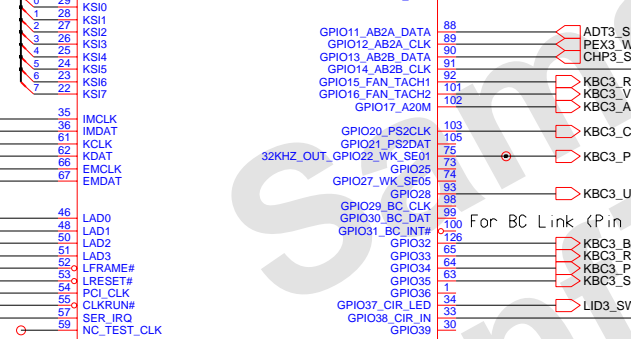
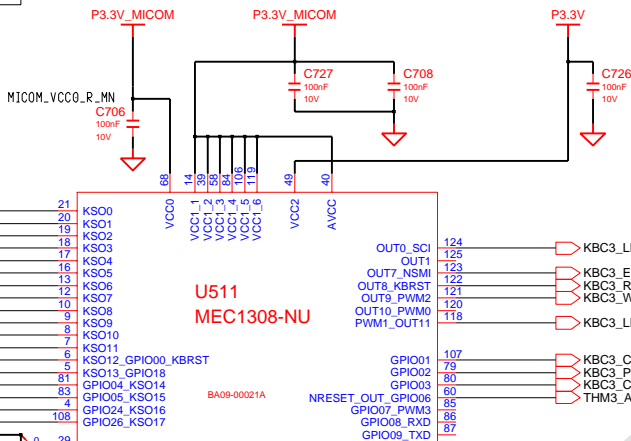
KBC3_L

KBC3_C

KBC3_P

KBC3_O

THM3_A

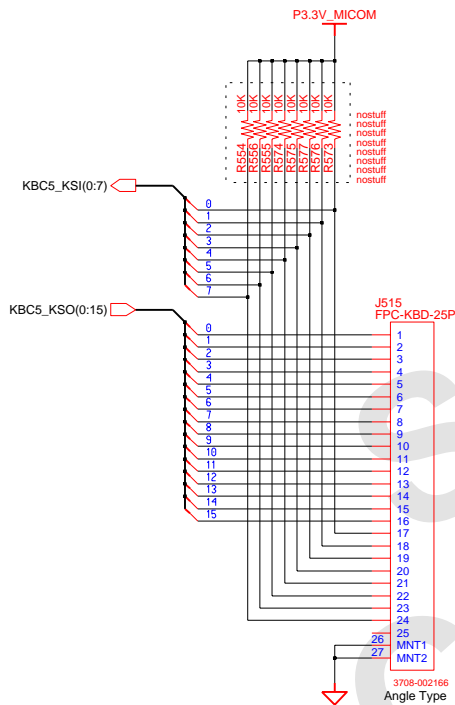


DESIGN	WK.YEO	DATE	7/13/2009	TITLE	STANFORD MAIN KEYBOARD CONTROLLER	SAMSUNG ELECTRONICS	
CHECK	SH.LEE	DEV. STEP	MP				
APPROVAL	KK.BIN	REV	1.0				
MODULE CODE	LAST EDIT		July 31, 2009 07:39:21 AM				PAGE

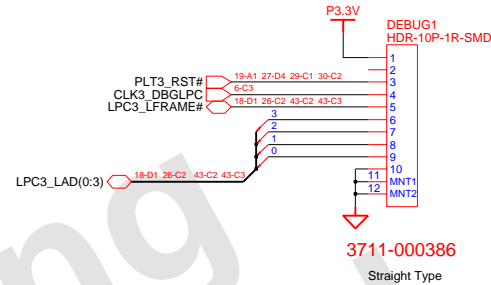
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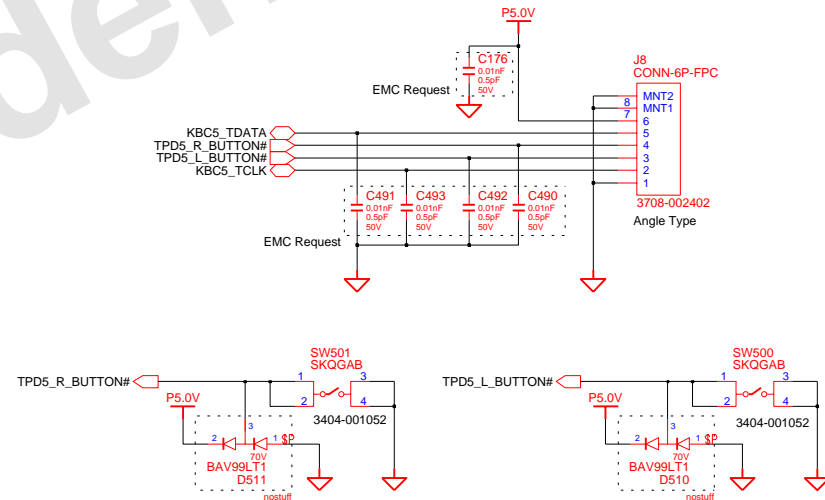
KEYBOARD



DEBUG PORT

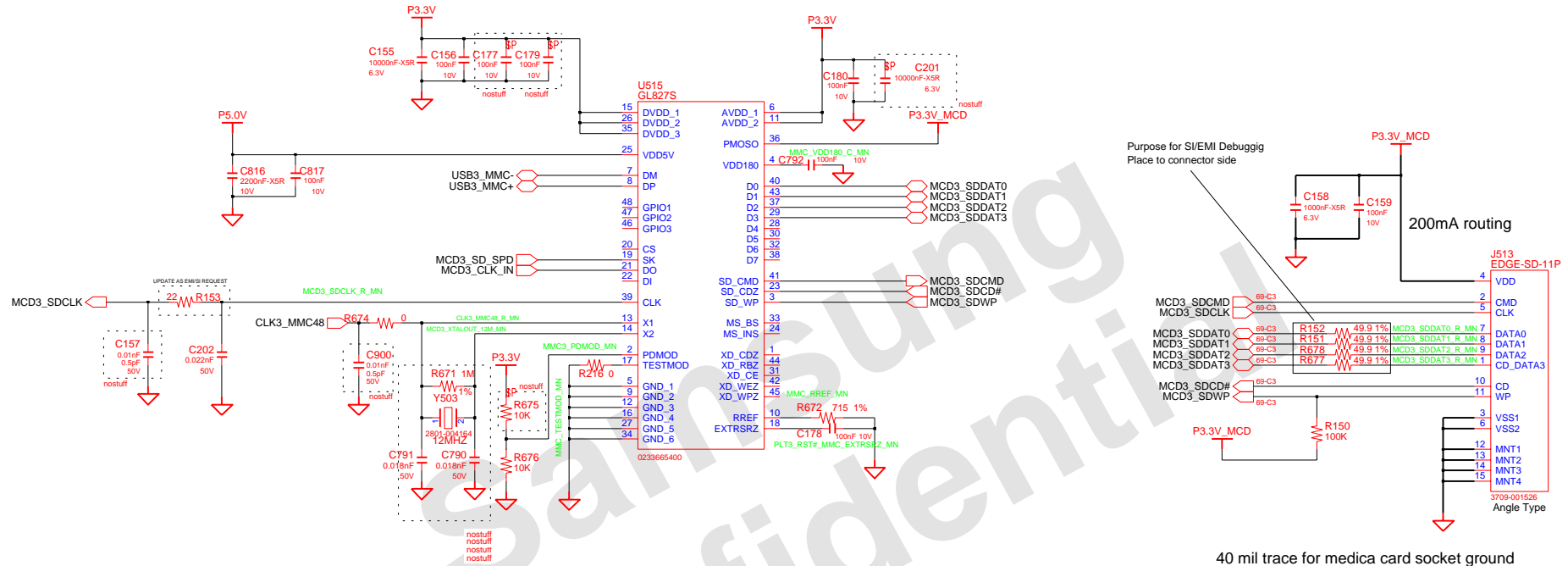


TOUCHPAD



DESIGN	WK.YEO	DATE	7/13/2009	TITLE	STANFORD MAIN MICOM GLUE LOGIC	SAMSUNG ELECTRONICS
CHECK	SH.LEE	DEV. STEP	MP			PART NO. BA41-0XXXXA
APPROVAL	KK.BIN	REV	1.0			
MODULE CODE		LAST EDIT	July 31, 2009 07:39:21 AM	PAGE	29	OF 47

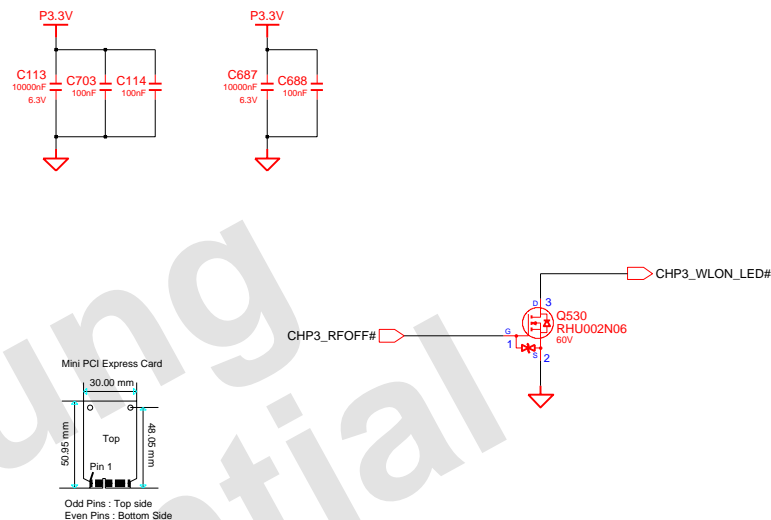
MMC



Power Down Mode	827S-05 and later
PU : No Stuff, PD : Stuff	Power Saving Mode Enable
PU : Stuff, PD : No Stuff	Remote Wake Up Enable

MCD3_SD_SPD	SD v1.0 Clock Option
PU / PD : No Stuff	24 MHz (default)
PU : Stuff, PD : No Stuff	15 MHz

MCD3_CLK_IN	827S Clock Source option
PU : X, PD : X	12MHz, fixed S/N
PU : No Stuff, PD : Stuff	12MHz, no S/N
PU : Stuff, PD : No Stuff	48MHz

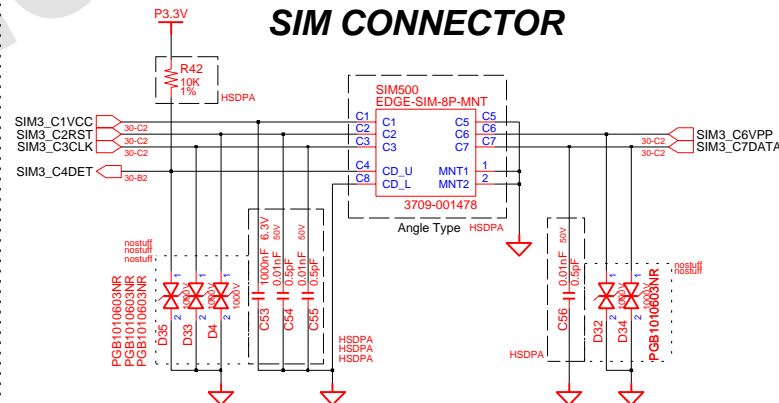


HSDPA, 4mm

The diagram illustrates the pin configuration and electrical connections for the Edge-MiniPCIE-E-52P connector. Key components and connections include:

- Power and Ground:** P3.3V and P1.5V planes are shown. Decoupling capacitors C705 (100nF) and C704 (100nF) are connected to the P1.5V plane. A 10K resistor R99 is connected to P3.3V.
- Signal Connections:**
 - PEX3_WAKE# (Pin 1)
 - IN3_CLKREQ#2 (Pin 3)
 - K1_MINIPCIE2# (Pin 5)
 - LK1_MINIPCIE2 (Pin 7)
 - PEX1_MINIRXN2 (Pin 19)
 - PEX1_MINIRXP2 (Pin 21)
 - PEX1_MINITXN2 (Pin 31)
 - PEX1_MINITXP2 (Pin 33)
 - USB3_MINIPCIE2- (Pin 45)
 - USB3_MINIPCIE2+ (Pin 47)
 - SIM3_C1VCC (Pin 30-B4)
 - SIM3_C7DATA (Pin 30-B3)
 - SIM3_C3CLK (Pin 30-B4)
 - SIM3_C2RST (Pin 30-B3)
 - SIM3_C6VPP (Pin 30-B3)
 - CHP3_3GDIFF# (Pin 0)
 - PLT3_RST# (Pin 0)
 - SIM3_C4DET (Pin 30-A4)
- Connector Details:** The connector is labeled J5 EDGE-MINI-PCIE-E-52P. The pin list on the right includes WAKE*, RSVD, CLKREQ*, REFCLK+, and various data and control lines for SIM and USB3.
- Scale:** A 1.5mm scale bar is provided at the bottom right.

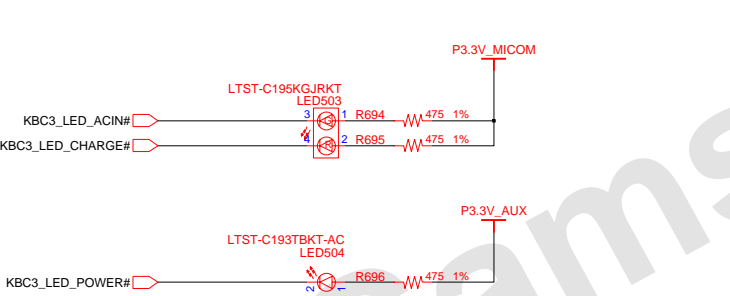
SIM CONNECTOR



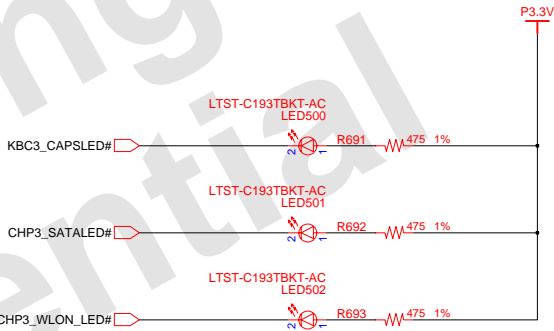
DESIGN	WK.YEO	DATE	7/13/2009	TITLE STANFORD MAIN WLAN & HSDPA	SAMSUNG ELECTRONICS	
CHECK	SH.LEE	DEV. STEP	MP			
APPROVAL	KK.BIN	REV	1.0			
MODULE CODE		LAST EDIT		July 31, 2009 07:39:21 AM	PAGE	32 OF 47

LED INTERFACE

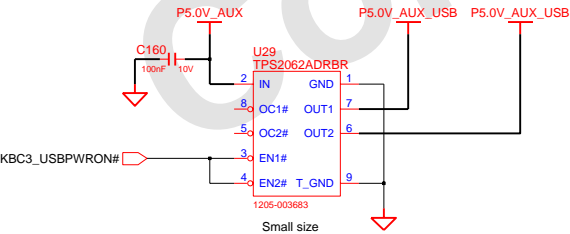
ADAPTER IN / CHARGING LED



FUNCTION KEY LEDS



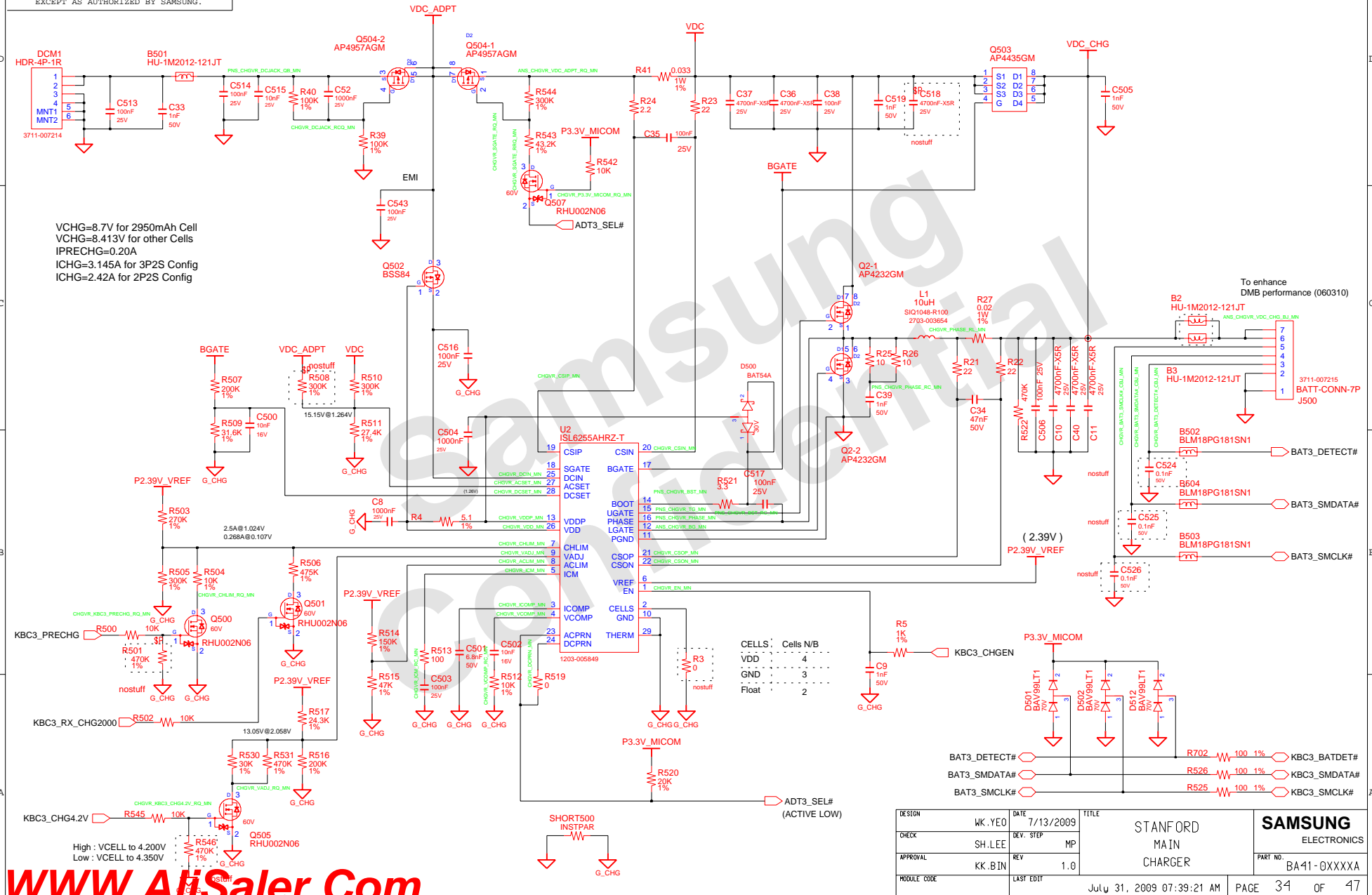
USB SUB BOARD POWER



DESIGN	WK.YEO	DATE	7/13/2009	TITLE	STANFORD MAIN LED I/F	SAMSUNG ELECTRONICS
CHECK	SH.LEE	DEV. STEP	MP			PART NO. BA41-0XXXXA
APPROVAL	KK.BIN	REV	1.0			
MODULE CODE		LAST EDIT	July 31, 2009 07:39:21 AM	PAGE	33	OF 47

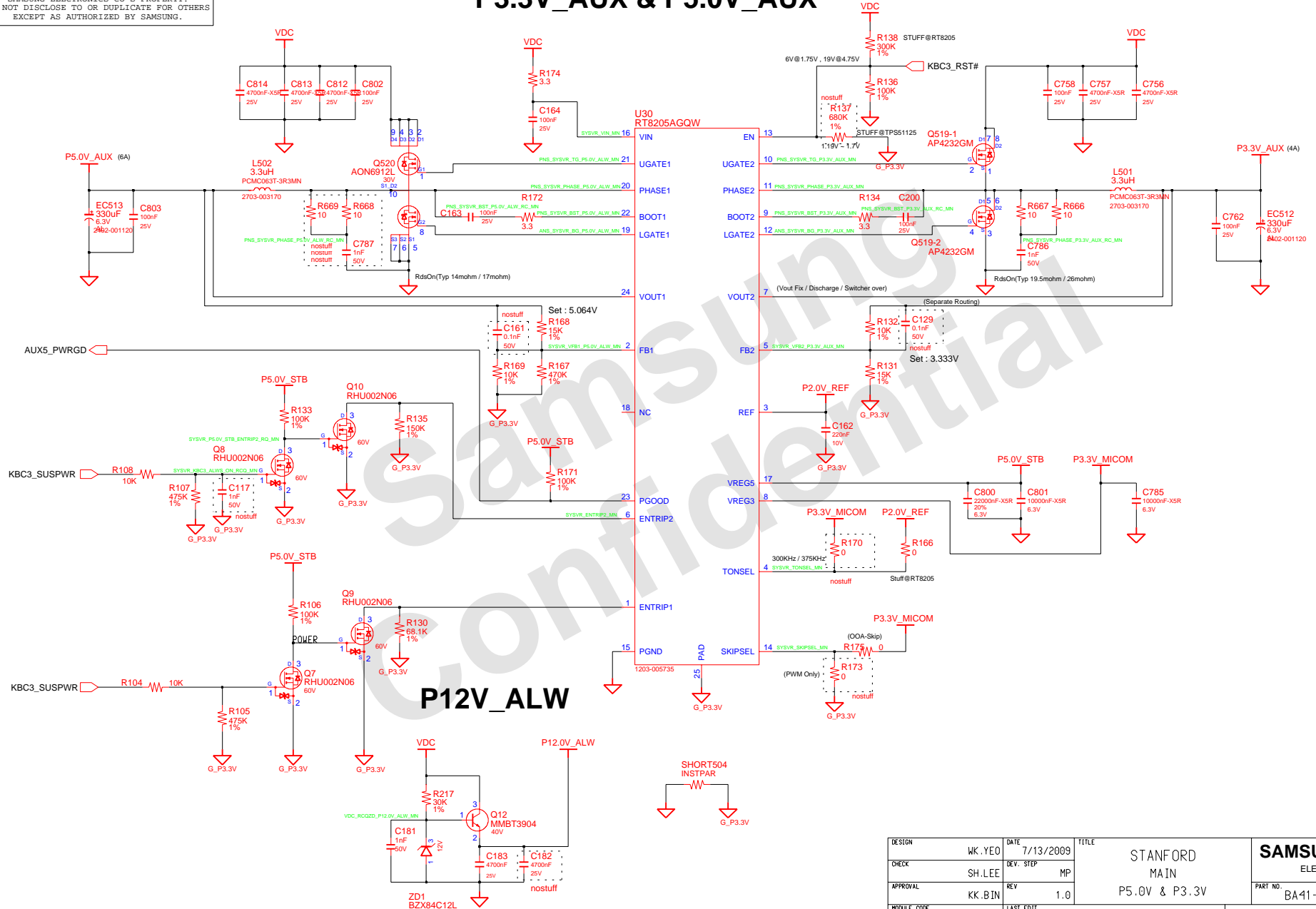
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CHARGER & POWER MANAGEMENT



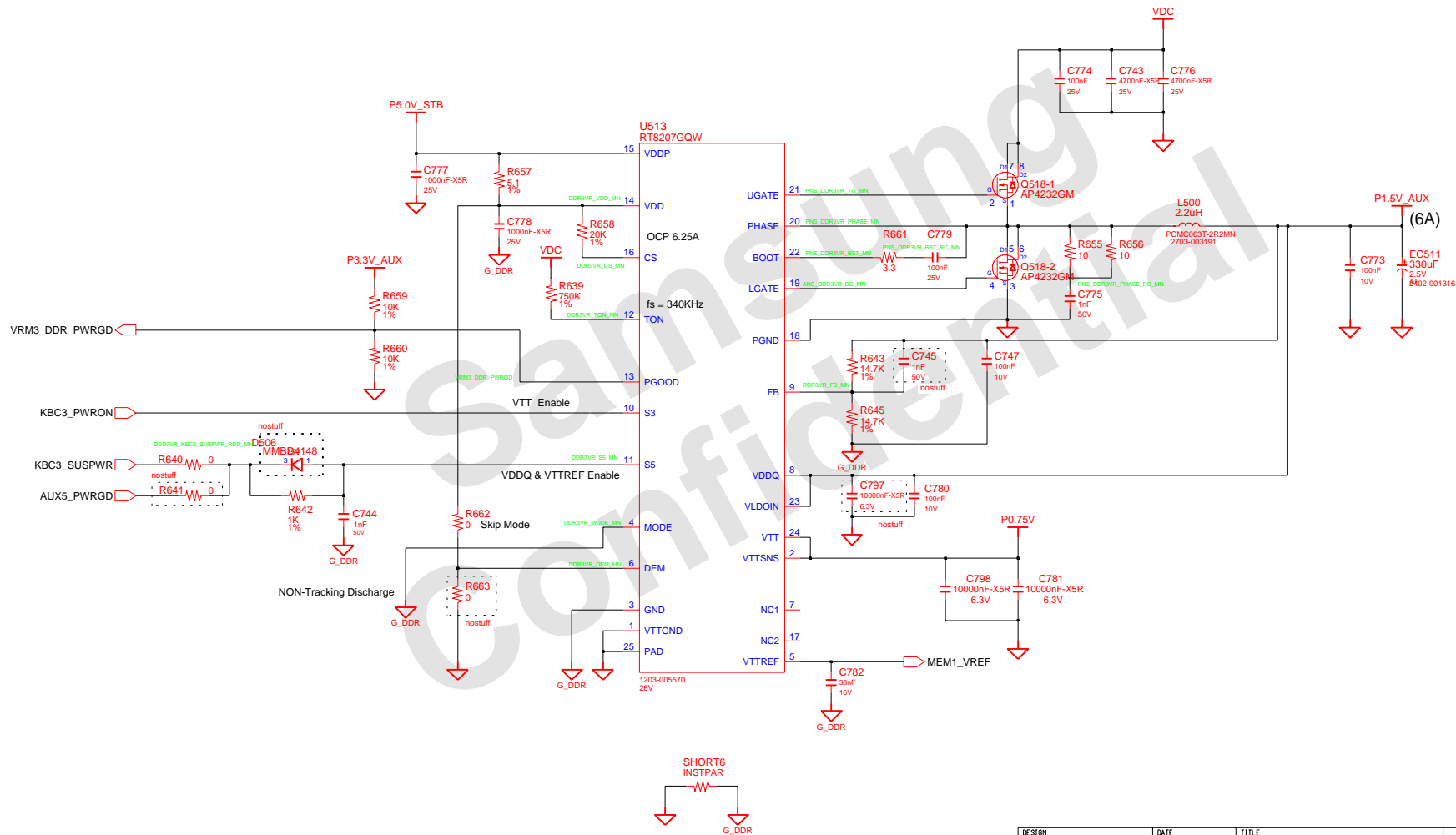
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P3.3V_AUX & P5.0V_AUX



DESIGN		WK.YE0		DATE		7/13/2009		TITLE				STANFORD MAIN				SAMSUNG ELECTRONICS			
CHECK		SH.LEE		DEV. STEP		MP													
APPROVAL		KK.BIN		REV		1.0		P5.0V & P3.3V				PART NO.				BA1-0XXXXA			
MODULE CODE				LAST EDIT								July 31, 2009 07:39:21 AM				PAGE		35	

DDR3 Power

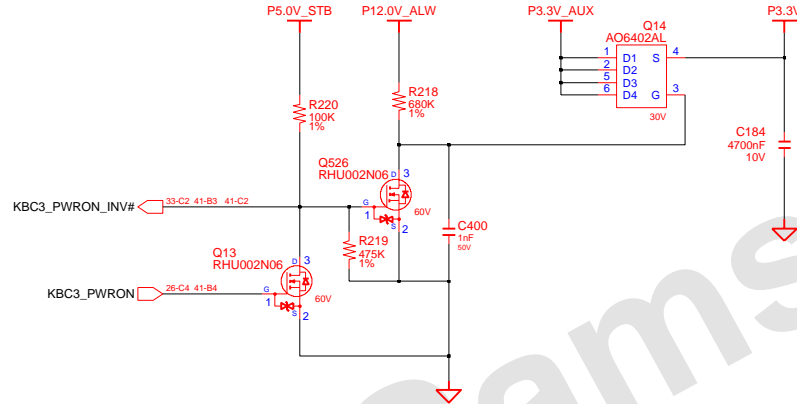


DESIGN	WK.YEO	DATE	7/13/2009	TITLE	STANFORD MAIN DDR3 POWER	SAMSUNG ELECTRONICS
CHECK	SH.LEE	DEV. STEP	MP			PART NO. BA41-0XXXXA
APPROVAL	KK.BIN	REV	1.0			
MODULE CODE		LAST EDIT	July 31, 2009 07:39:21 AM	PAGE	36	OF 47

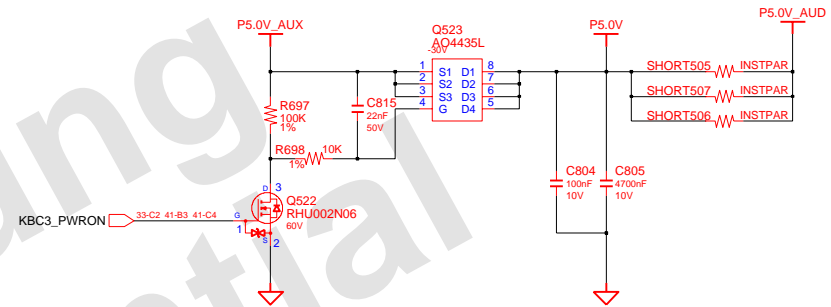
DESIGN	WK.YEO	DATE	7/13/2009	TITLE		STANFORD MAIN P1.05V		SAMSUNG ELECTRONICS	
CHECK	SH.LEE	DEV. STEP	MP						
APPROVAL	KK.BIN	REV	1.0	PART NO.		BA41-0XXXXA			
MODULE CODE	LAST EDIT								
				July 31, 2009 07:39:21 AM		PAGE	37	OF	47

SWITCHED POWER

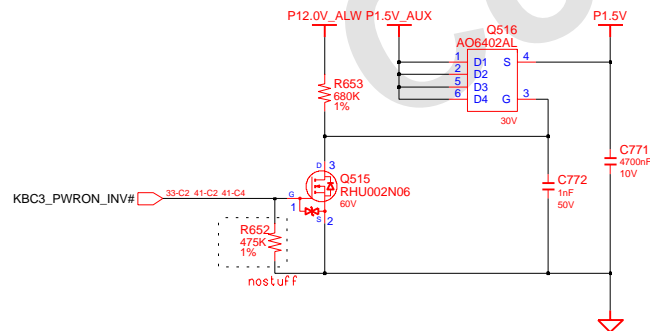
Switched Power On (P3.3V)



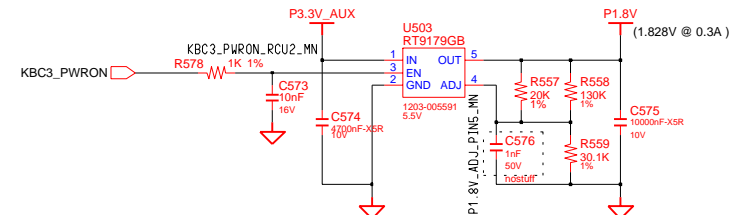
Switched Power On (P5V)



Switched Power On (P1.5V)

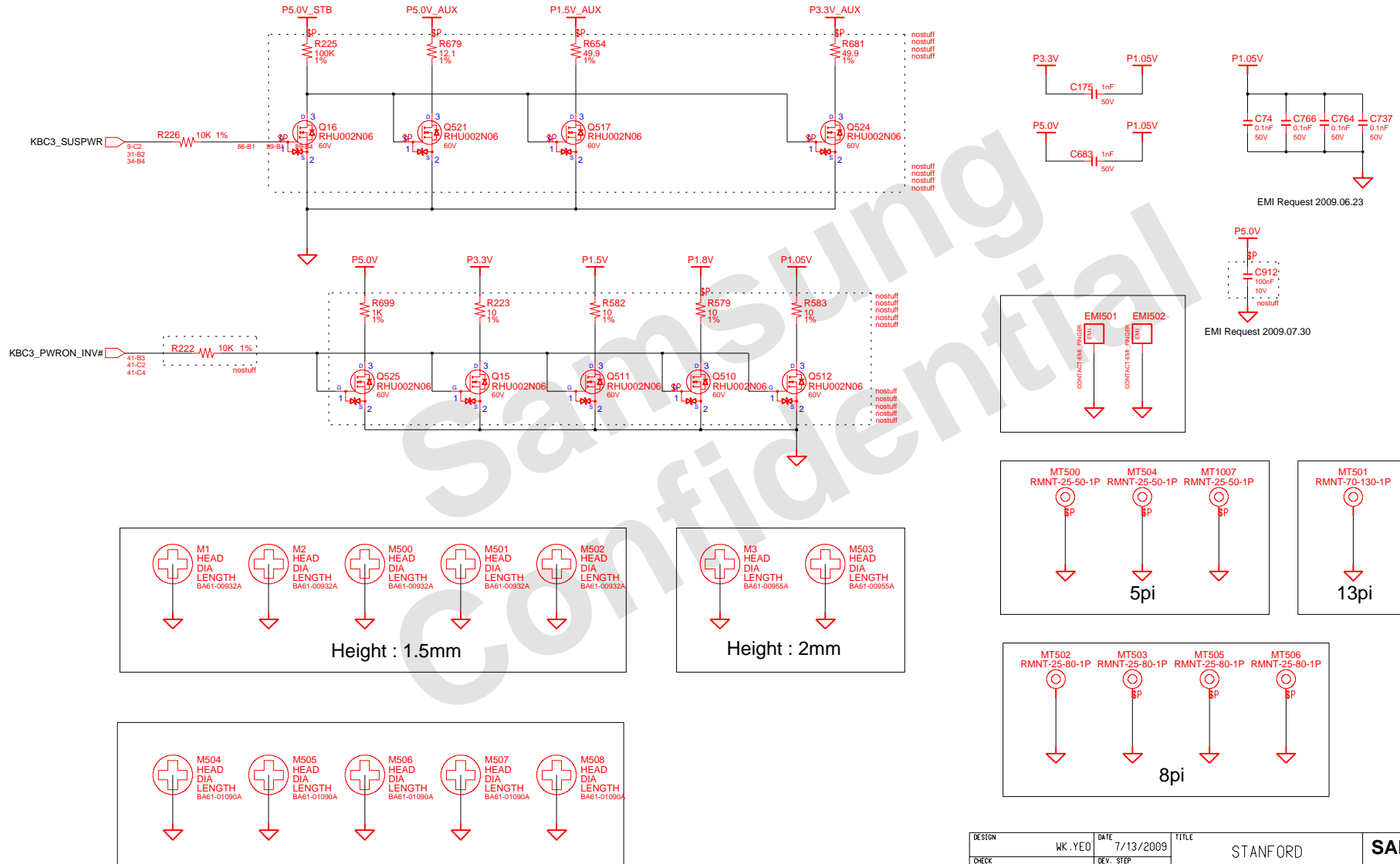


P1.8V



DESIGN	WK.YEO	DATE	7/13/2009	TITLE	STANFORD MAIN SWITCHED POWER	SAMSUNG ELECTRONICS PART NO. BA41-0XXXXA
CHECK	SH.LEE	DEV. STEP	MP			
APPROVAL	KK.BIN	REV	1.0			
MODULE CODE		LAST EDIT	July 31, 2009 07:39:21 AM	PAGE	39 OF 47	

DISCHARGE



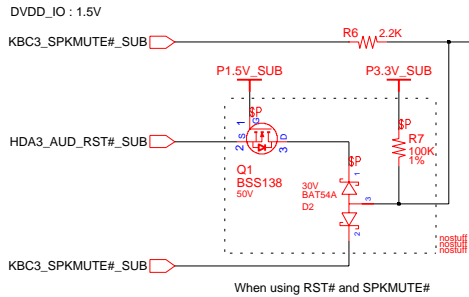
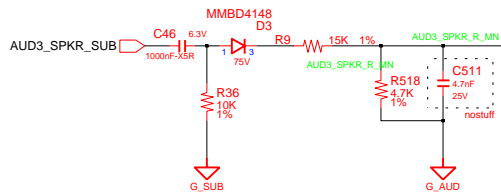
DESIGN	WK.YEO	DATE	7/13/2009	TITLE	STANFORD MAIN DISCHARGER	SAMSUNG ELECTRONICS
CHECK	SH.LEE	DEV. STEP	MP			PART NO. BA41-0XXXXA
APPROVAL	KK.BIN	REV	1.0			
MODULE CODE		LAST EDIT	July 31, 2009 07:39:21 AM	PAGE	40	OF 47

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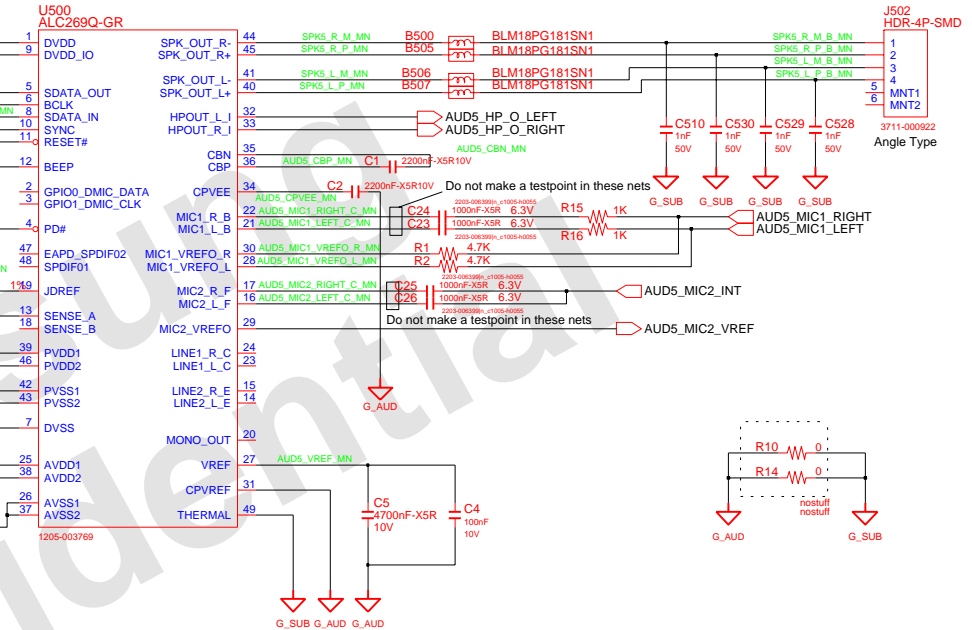
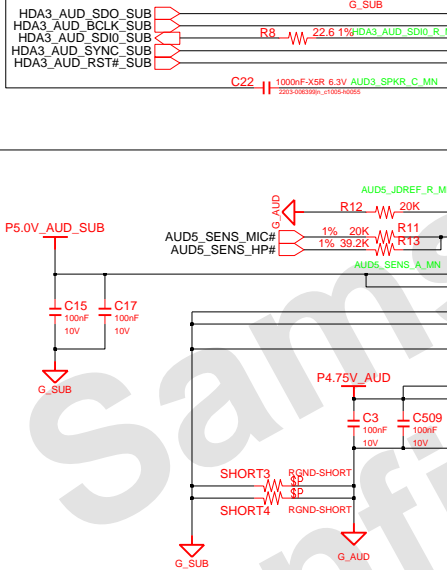
Codec Pin9 Setting	
S/B with Low Voltage IO	S/B without Low Voltage IO
Pin9 : 1.5V	Pin9 : 3.3V

Audio Sub Board

SMD_A : 3711-000922
SMD_S : 3711-000456

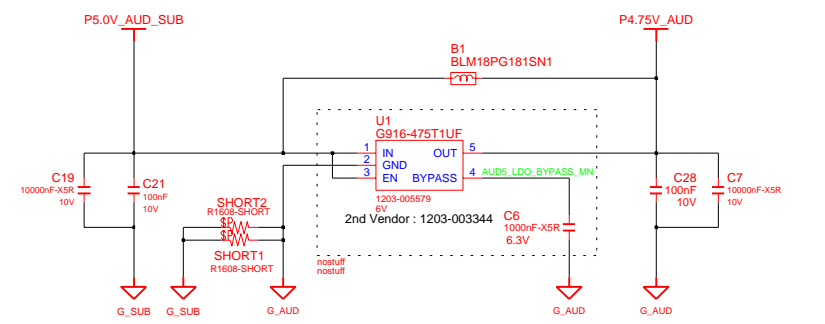
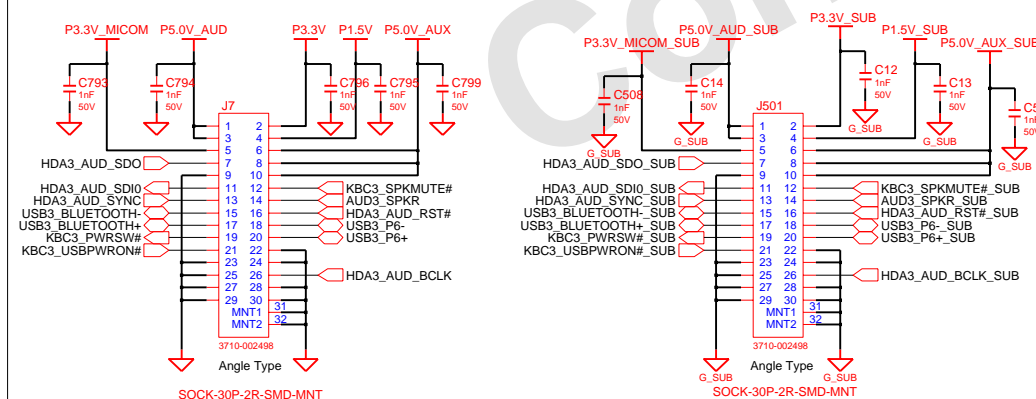


When using RST# and SPKMUTE#



< MAIN TO SUB >

< SUB TO MAIN >

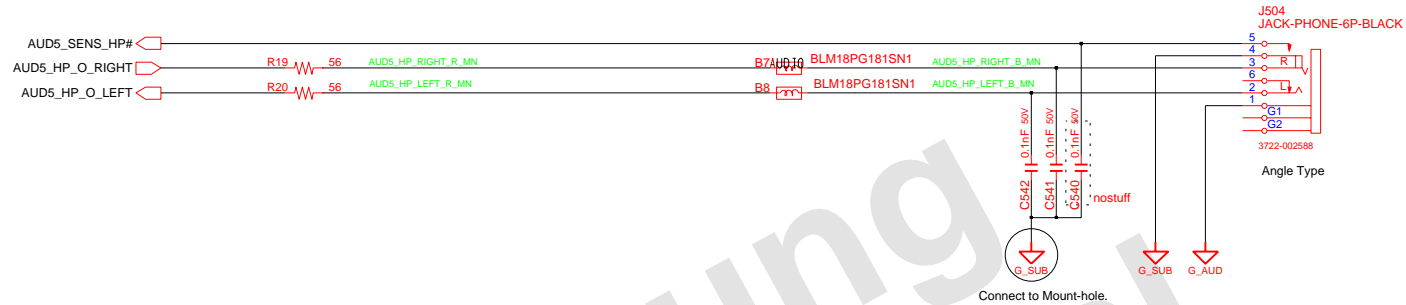


DESIGN	WK.YEO	DATE	7/13/2009	TITLE	STANFORD MAIN AUDIO SUB-BOARD	SAMSUNG ELECTRONICS
CHECK	SH.LEE	DEV. STEP	MP	REV	1.0	PART NO. BA41-0XXXXA
APPROVAL	KK.BIN	LAST EDIT	July 31, 2009 07:39:21 AM	PAGE	41	OF 47

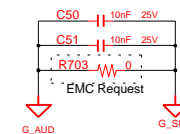
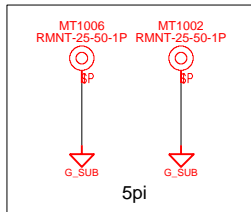
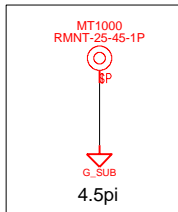
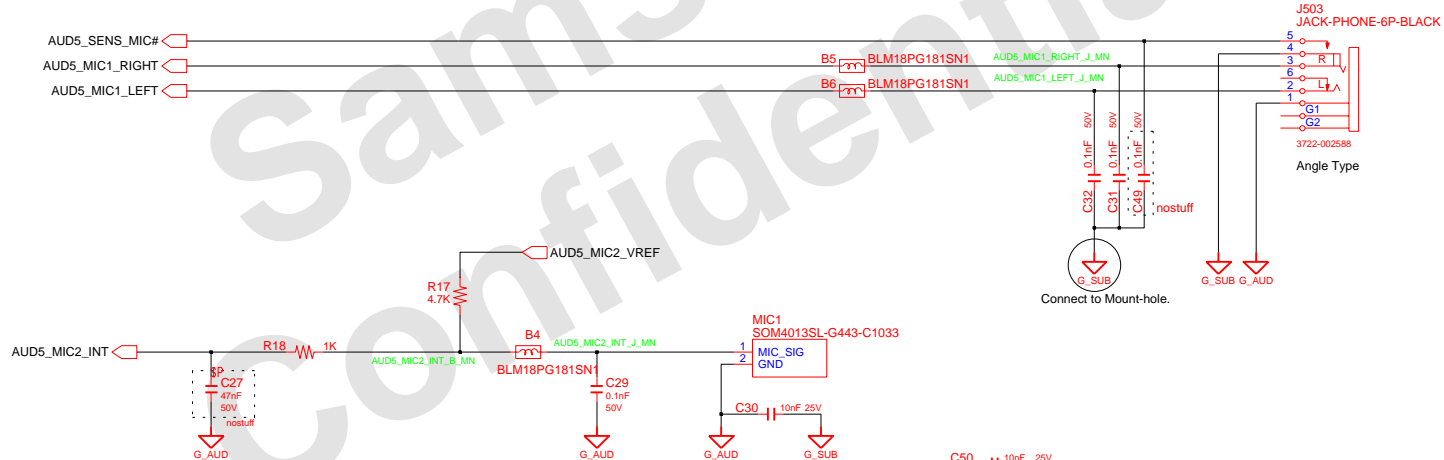
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HEADPHONE



MIC JACK

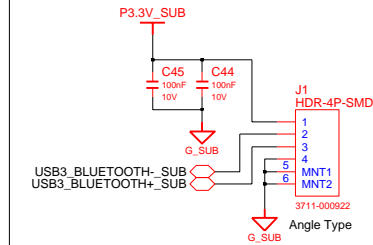


DESIGN	WK.YEO	DATE	7/13/2009	TITLE	STANFORD MAIN AUDIO SUB-BOARD	SAMSUNG ELECTRONICS
CHECK	SH.LEE	DEV. STEP	MP			PART NO. BA41-0XXXXA
APPROVAL	KK.BIN	REV	1.0			
MODULE CODE		LAST EDIT	July 31, 2009 07:39:21 AM	PAGE	42	OF 47

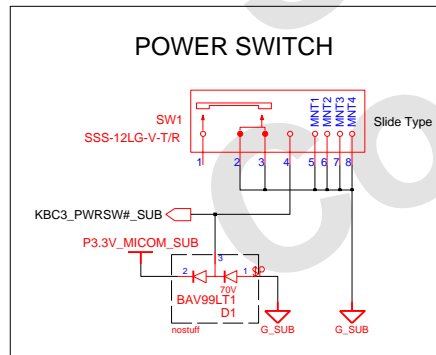
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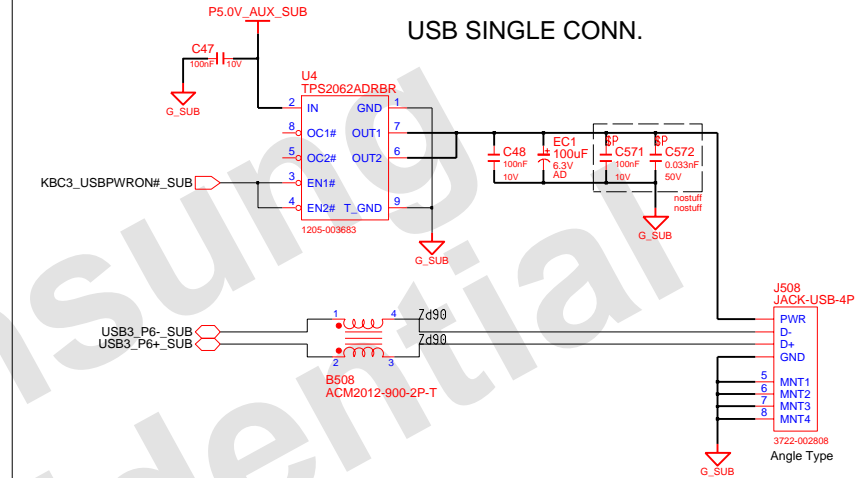
BLUETOOTH



POWER SWITCH



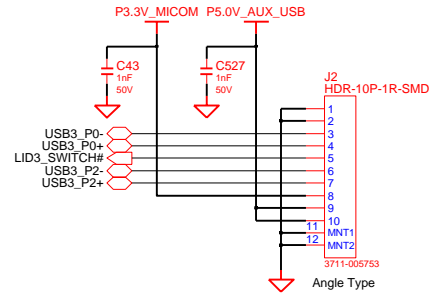
USB SINGLE CONN.



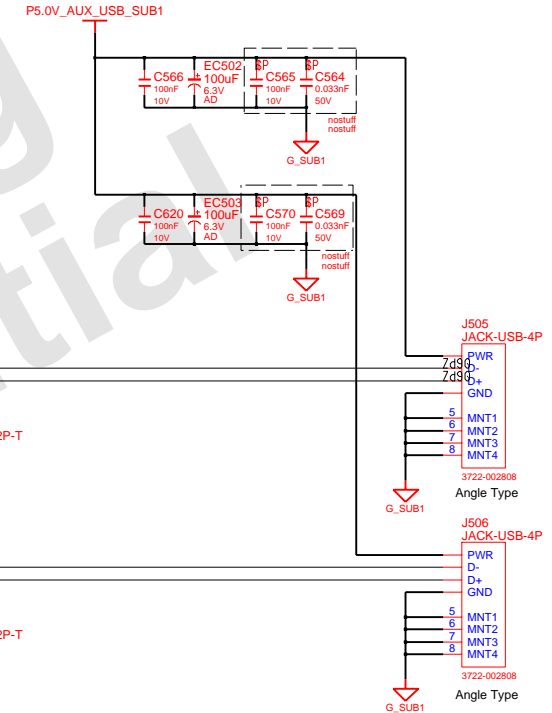
DESIGN	WK.YEO	DATE	7/13/2009	TITLE	STANFORD MAIN AUDIO SUB-BOARD	SAMSUNG ELECTRONICS
CHECK	SH.LEE	DEV. STEP	MP			PART NO. BA41-0XXXXA
APPROVAL	KK.BIN	REV	1.0			
MODULE CODE		LAST EDIT	July 31, 2009 07:39:21 AM	PAGE	43	OF 47

USB SUB BOARD

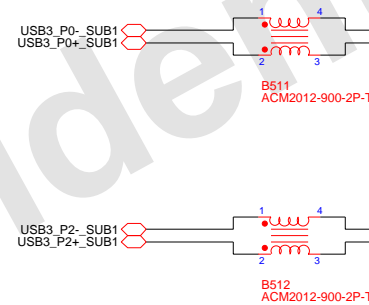
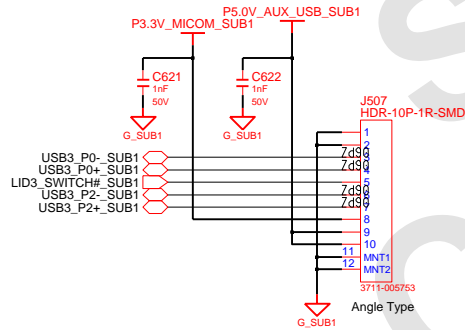
MAIN TO USB SUB BOARD



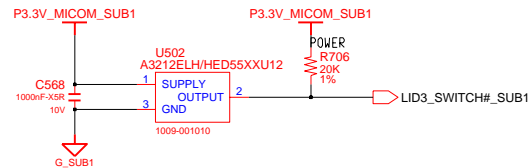
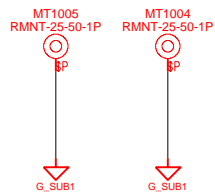
USB SINGLE CONN.



USB SUB BOARD TO MAIN

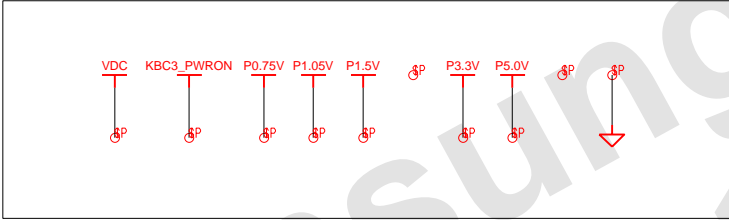


LID_SWITCH



DESIGN	WK.YEO	DATE	7/13/2009	TITLE	STANFORD MAIN USB SUB-BOARD	SAMSUNG ELECTRONICS
CHECK	SH.LEE	DEV. STEP	MP			PART NO. BA41-0XXXXA
APPROVAL	KK.BIN	REV	1.0			
MODULE CODE		LAST EDIT	July 31, 2009 07:39:21 AM	PAGE	44	OF 47

FOR ICT



* ADD GUIDE HOLE BEFORE #1PIN

#1 PIN	VDC
#2 PIN	POWER_ON_SIGNAL
#3 PIN	P0.75V
#4 PIN	P1.05V
#5 PIN	P1.5V
#6 PIN	P1.8V (reserved)
#7 PIN	P3.3V
#8 PIN	P5.0V
#9 PIN	RESERVED
#10 PIN	GROUND

* ADD GUIDE HOLE AFTER #10PIN

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CHECK	SH.LEE	DEV. STEP	MP		
APPROVAL	KK.BIN	REV	1.0		
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